

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MANISHA AGARWALA,
LEWIS NARDINI, and TIMOTHY D. ANDERSON

Appeal 2008-1134
Application 10/301,886
Technology Center 2100

Decided: September 23, 2008

Before KENNETH W. HAIRSTON, JOSEPH F. RUGGIERO,
and MARC S. HOFF, *Administrative Patent Judges*.

RUGGIERO, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Final Rejection of
claims 1-3. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellants' invention relates to producing trace data for a data processor in which the operation of the data processor is paused in response to an emulation halt command. An exception signal is generated in response to an emulation change in the data processor program counter and is supplied to the program counter data trace stream. (Spec. 12-13).

Claim 1 is illustrative of the invention and reads as follows:

1. A method of producing trace data for a data processor comprising the steps of:

pausing operation of the data processor in response to an emulation halt command;

generating a unique exception signal in response to an emulation change in a program counter of the data processor during an emulation halt; and

supplying the unique exception signal to a program counter trace data stream for the data processor.

The Examiner relies on the following prior art reference to show unpatentability:

Rana

US 6,314,529 B1

Nov. 6, 2001

Claims 1-3, all of the appealed claims, stand rejected under 35 U.S.C § 102(b) as being anticipated by Rana.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs and Answer for the respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed waived [see 37 C.F.R. § 41.37(c)(1)(vii)].

ISSUE

Under 35 U.S.C § 102(b), does Rana have a disclosure which anticipates the invention set forth in appealed claims 1-3?

PRINCIPLES OF LAW

It is axiomatic that anticipation of a claim under § 102 can be found if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992). Anticipation of a patent claim requires a finding that the claim at issue “reads on” a prior art reference. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed. Cir. 1999) (“In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.”) (internal citations omitted).

ANALYSIS

With respect to the 35 U.S.C. § 102(b) rejection of independent claim 1 based on Rana, the Examiner indicates (Ans. 3) how the various

limitations are read on the disclosure of Rana. In particular, the Examiner directs attention to the portions of the disclosure of Rana at column 9, lines 48-52 and 54-58, and column 10, lines 12-13, as well as the illustration at Figure 2 of Rana.

Appellants' arguments in response assert that the Examiner has not shown how each of the claimed features is present in the disclosure of Rana so as to establish a prima facie case of anticipation. Appellants' arguments initially focus on the contention that, in addressing the language of independent claim 1 which requires an emulation change in a program counter, the Examiner has erred in identifying the trace counter 64 in Rana as the element which corresponds to the claimed program counter.

We agree with Appellants. As asserted by Appellants (App. Br. 6-7; Reply Br. 4-5), a skilled artisan would recognize a program counter as an element which steps through addresses of instructions to be executed by a data processor as opposed to the trace counter 64 described by Rana (col. 9, ll. 7-15), which merely provides signals which determine the address locations in trace memory 12 where signals from the emulation circuit 40 are to be stored.

Further, aside from a lack of a disclosure of a program counter as claimed, we find that the Examiner erred in finding that Rana discloses the generation of an exception signal "in response to an emulation change in a program counter of the data processor during an emulation halt" as set forth in appealed claim 1. Even assuming the trace counter 64 in Rana could somehow be considered a program counter, we find that, while the Examiner has identified the signals "trace, skip trace, break, etc." in Rana as corresponding to the claimed "exception" signals, these signals are used by

Rana to effect an emulation change in the “program” counter as opposed to being generated in response to an emulation change in the “program” counter.

We recognize that the Examiner, at page 5 of the Answer, has further explained the stated position with regard to Rana’s disclosure of the generation of an exception signal by contending that emulation circuit 40 provides such an exception signal to the trace counter 64 in trace control element 52 when the operation of the emulation circuit is halted. We do not find any disclosure in Rana, nor has the Examiner identified any, to support such a conclusion.

Lastly, we additionally find no disclosure in Rana which corresponds to the claimed feature of applying the generated exception signal to the program counter trace data stream. The Examiner (Ans. 8) has posited that based upon the generation of signals, such as “skip trace” and “break”, the “program” counter 64 in Rana would not be incremented, thereby satisfying the claimed requirement that the generated exception signal is applied to the program counter trace data stream. For the Examiner’s position to have any merit, the output of “program counter” would have to be considered a trace data stream. As argued by Appellants (App. Br. 8; Reply Br. 5-7), however, the addresses that are output from counter element 64 in Rana are not being traced but, rather, it is the address signals applied to the monitored memory 30 that are being traced.

In view of the above discussion, we find that the Examiner erred in concluding that all of the claimed limitations are present in the disclosure of Rana. We, therefore, do not sustain the Examiner’s 35 U.S.C. § 102(b) rejection of independent claim 1, nor of claims 2 and 3 dependent thereon.

Appeal 2008-1134
Application 10/301,886

CONCLUSION

In summary, we have not sustained the Examiner's 35 U.S.C. § 102(b) rejection of any of the claims on appeal. Therefore, the decision of the Examiner rejecting claims 1-3 is reversed.

REVERSED

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