

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte RENE J. GLAISE, FRANCOIS KERMAREC,  
ERIC LALLEMAND, TAN PHAM, HANS R. SCHINDLER,

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Appeal No. 2000-0372  
Application No. 08/421,338

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ON BRIEF

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Before KRASS, BARRETT and RUGGIERO, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-4 and 6-10. The examiner withdrew the rejection of claim 5.

The invention is directed to a swapping function. More particularly, the invention is used in communication systems wherein input values are headers of data streams

received by the system and output values are headers of corresponding data streams transmitted by the communication system. It is desirable to change the input value into the corresponding or related output value and the invention is directed to performing this task faster by establishing, or following, a unique path, identified by the input variable, in sequence through a plurality of cascaded memories to a unique storage location which contains the desired corresponding output value.

Independent claim 1 is reproduced as follows:

1. An apparatus for providing output values corresponding to a number  $E$  of  $n$ -bit input values, with  $E$  being an integer lower or equal to  $2^p - 1$ , characterized in that it comprises:

- a plurality of cascaded random access memories (24-A, 24-B and 24-C) having a  $2^d$  addressing capability, where  $d$  is an integer higher than  $p$ ,

- means for storing in each random access memory  $p$ -bit pointers, each one of them being different from the others and being assigned to one input value,

- means (40, 122 to 158) for sequentially addressing and reading at least one of the random access memories, the first one being addressed with a part including a number  $n_1$  of bits of the input value, with  $n_1$  equal or lower than  $d$ , and each one of the next memories being addressed with the pointer read from the preceding memory concatenated with a part including a number  $n_i$  of bits of the input value, with  $n_i$  equal to or lower than  $n - n_1$ ,

- means (40, 160) for finding the output value as a result of the addressing of the last random access memory in the sequence.

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The examiner relies on the following references:

Dujari	4,984,151	Jan. 08, 1991
Stewart	EP 500,238	Aug. 26, 1992

Claims 1-4 and 6-10 stand rejected under 35 U.S.C. § 103 as unpatentable over Stewart in view of Dujari.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

#### OPINION

Stewart is directed to a header translation unit for an asynchronous transfer mode [ATM] switching system, similar to appellants'. In Stewart, a content addressable memory [CAM] is used to effect a mapping function between a plurality of logical addresses and a plurality of physical addresses. CAM 5 is under the control of control unit 6. When a data cell is received on line 2, Policing and Header Translation Unit [PHTU] 1 extracts the virtual path identifier [VPI] and virtual channel identifier [VCI] fields from the ATM cell header. CAM 5 is then searched for these two fields to see if a match can be found. If matching values are found, CAM 5 provides an output signal on line 9 corresponding to the physical address for the particular match for storage in RAM 8. PHTU 1 has the function of translating the incoming ATM cell data into a form which can be switched by a switch network

The examiner contends that Stewart's RAM table is "functionally equivalent" to the cascaded RAM of the instant claims because "it also stores the input data and has a capability of addressing  $2^d$  bits" [answer-page 4]. The examiner takes the position that Stewart does not teach the claimed means for sequentially addressing and reading the random access memories but, instead, uses a search method to perform the sequential addressing and reading of the memory. Thus, the examiner turns to Dujari for a method of sequential addressing and reading using pointers, identifying, in the abstract, column 1, lines 40+, column 2, lines 28+, and column 7, lines 40-65, the calculation of a next address by adding/concatenating a base address ( $n_1$ ) with an offset ( $n_i$ ). The examiner then concludes that it would have been obvious to use Dujari's table walking/search process in Stewart's header swapping device to search for the correct physical address to swap in order to "improve the efficiency of the addressing and reading process of Stewart's, who also teaches searching through a table for the correct address. The function of the means for finding the output value as a result of the addressing of the random access memory is taught by Stewart through performing the search for the physical address in the memory and outputting it (column 2 lines 40-50)" [answer-page 5].

Appellants contend that the function of Stewart's RAM TABLES 8 is identical to the control block storage in the upper portion of memory 24-A of the instant application but is unrelated to the cascaded memories disclosed and claimed by appellants. The cascaded memories are used to sequentially provide a plurality of addresses, the last one identifying the location of the control block in the upper portion of memory 24-A which includes the corresponding value. Appellants disagree with the examiner that Stewart teaches a cascaded memory as a CAM to map between logical and physical addresses and that the RAM table of Stewart is functionally equivalent to the cascaded RAM [principal brief-page 6]. Appellants also question how or why artisans would have modified anything in Stewart with the teachings of Dujari.

We agree with appellants that there is nothing in Stewart that would indicate that Stewart's RAM table is "functionally equivalent" to the claimed cascaded random access memories. The telling error in the examiner's position is brought out by the examiner's response to appellants' argument, at page 6 of the answer. The examiner states thereat that "Stewart teaches a content addressable memory (CAM) which performs the same function as the claimed cascaded random access memory, storing data. Therefore, the Examiner contends that the CAM is an equivalence as the cascaded random access memories."

On its face, the examiner has failed to present a prima facie case of obviousness of the claimed subject matter since many patentably distinct inventions perform the “same function.” However, the particular mechanism by which that function is performed may patentably distinguish over other devices performing the same function in a different and unobvious manner. Thus, it is the examiner’s burden to show that the claimed cascaded memories are taught or suggested by either Stewart or Dujari or the combination thereof.

Claim 1 calls for, inter alia, a plurality of cascaded random access memories. In each memory is stored “p-bit pointers” with each pointer being different from the others and being assigned one input value. The means for sequentially addressing and reading the random access memories does so by addressing a first memory with a part including a number  $n_1$  of bits of the input value and each one of the next memories being addressed is addressed with a pointer read from the preceding memory concatenated with a part including a number  $n_i$  of bits of the input value, with  $n_i$  being equal to or lower than  $n_{i-1}$ . We find nothing in the applied references which suggests such cascaded random access memories or the addressing scheme claimed. We agree with appellants that since “neither the structure or operation of the...RAM TABLES 8 is described by Stewart, the assignment of any physical and/or functional attributes to it would amount to no more than speculation” [principal brief-page 6]. A conclusion of obviousness under 35 U.S.C. §103 cannot be based on speculation.

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Accordingly, we will not sustain the rejection of claim 1, or of claims 2-4 and 6-10 dependent thereon, under 35 U.S.C. § 103.

The examiner's decision is reversed.

REVERSED

ERROL A. KRASS	)	
Administrative Patent Judge	)	
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	)	BOARD OF PATENT
LEE E. BARRETT	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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JOSEPH F. RUGGIERO	)	
Administrative Patent Judge	)	

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