

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte THOMAS MICHAEL ALBERS, JOHN VERNON EBERST,
DARWIN FONTENOT, RICHARD LYNN PYRA,
MARK WILLIAM WELKER, PAUL BERTON WOOD, and
JACK E. BRESENHAM

Appeal No. 2000-0414
Application No. 08/811,101

ON BRIEF

Before KRASS, JERRY SMITH, and DIXON, **Administrative Patent Judges**.
DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 and 24-35, which are all of the claims pending in this application.

We REVERSE.

BACKGROUND

The appellants' invention relates to a video graphics controller with high speed line draw processor. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

1. A graphics device comprising:
 - a first register storing a first value indicative of the coordinates of a first endpoint of a line;
 - a second register storing a second value indicative of the coordinates of a second endpoint of the line;
 - clock circuitry including a clock signal which includes a plurality of clock cycles;
 - a command register for storing control bits;
 - a line draw engine coupled to receive the clock signal and at least one control bit from the command register, the line draw engine to generate line data based on said first and second values, the generation of line data beginning in the clock cycle immediately succeeding a clock cycle in which the second value is stored in the second register; and
 - a datapath circuitry including a graphics device output node for coupling to a memory, the datapath circuitry including a mask signal input.

The prior art reference of record relied upon by the examiner in rejecting the appealed claims is:

Miyashita et al. (Miyashita)

5,068,802

Nov. 26, 1991

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Claims 1 and 24-35 stand rejected under 35 U.S.C. § 103 as being unpatentable over Miyashita.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 15, mailed Feb. 19, 1999) for the examiner's reasoning in support of the rejections, and to appellants' brief¹ (Paper No. 14, filed Sep. 28, 1998) and reply brief (Paper No. 18, filed Mar. 15, 1999) for appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to appellants' specification and claims, to the applied prior art reference, and to the respective positions articulated by appellants and the examiner. As a consequence of our review, we make the determinations which follow.

Appellants argue that the examiner's rejection cannot be valid because the analysis is based upon flawed interpretation of the Miyashita reference. (See brief at page 7.) We agree with appellants. The examiner admits that Miyashita does not teach the generation of the line data beginning the clock cycle immediately succeeding a clock cycle, but relies upon the flow diagram in Figure 6 which the examiner maintains "suggests the starting of the line draw process immediate[ly] after finishing [the] input

¹ We note that appellants attached an unsigned proposed amendment to the appeal brief, but chose not to officially file the paper. Therefore, we decide the appeal on the claims as previously amended.

[of the] second value (steps 108-114)". (Examiner's answer, page 3). We disagree with the examiner. From our understanding of Figure 6 of Miyashita, Miyashita discloses that the inquiry concerning the use of the auto-adjust of input coordinates (step 112) takes place immediately after the input of the coordinates. Therefore, Miyashita would not suggest the starting of the line draw process immediately after finishing the input of the second value due to this intermediate step/inquiry. The examiner provides no further explanation or analysis of the teachings of Miyashita beyond stating that "[a]fter storing the value, the system will start to process the data in which that clock cycle is kicked in." (See answer at page 4.) Again, we disagree with the examiner's conclusion and do not find it to be supported by the teachings or suggestions in Miyashita, nor has the examiner established a convincing line of reasoning to support this conclusion. Therefore, we will not sustain the rejection of independent claim 1 and its dependent claims 24-26. Similarly, independent claim 27 contains similar limitations, and we will not sustain the rejection of claims 27-32.

With respect to independent claim 33, the examiner maintains that this claim is similar to the other rejected claims and does not provide further explanation of the rejection. (See answer at pages 3 and 6.) We disagree with the examiner. Appellants argue that the examiner has provided no indication of how this particular claim would be unpatentable in view of Miyashita. (See brief at page 11.) We agree with appellants. Appellants argue that the claimed invention recites the use of a command bit register

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and use thereof to automatically start the generation of the line data during the second time period. (See brief at page 11.) Appellants argue that the examiner has provided no teaching or discussion of the use of a start control bit. We agree with appellants, and find that the examiner has not established a *prima facie* case of obviousness with respect to independent claim 33 and dependent claims 34 and 35. Therefore, we will not sustain the rejection of claims 33-35.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1 and 24-35 under 35 U.S.C. § 103 is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	
)	BOARD OF PATENT
JERRY SMITH)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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JOSEPH L. DIXON)	
Administrative Patent Judge)	

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