

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KEIKO HAYAMI

Appeal No. 2000-0424
Application 08/760,510¹

ON BRIEF

Before KRASS, BARRETT, and SAADAT, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

¹ Application for patent filed December 5, 1996, entitled "Laminate Printed Circuit Board with Leads for Plating," which is claims the foreign filing priority benefit under 35 U.S.C. § 119 of Japanese Application 317689, filed December 6, 1995.

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DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 4 and 8, the only claims pending.

We reverse.

BACKGROUND

The invention relates to a laminate printed circuit board having a lead for plating. The problem with leads for plating in the prior art shown in Figs. 2A and 2B was that when the leads 3 were cut off after plating, the residual portions 4 were deformed and were apt to short-circuit nearby terminals. The problem is solved by using a single lead on the printed circuit board connected to the terminals to be plated and then disconnecting the terminals from each other by a hole through the lead. Claim 4 is directed to the embodiment of Figs. 3A-3C and claim 8 is directed to the embodiment of Figs. 4A and 4B.

Claim 4, which is directed to the embodiment of
Figs. 3A-3C, is reproduced below.²

4. A laminate printed circuit board, comprising:

a plurality of plated conductors provided on said laminate printed circuit board, each of said conductors extending in a first direction and toward an edge of said printed circuit board;

a plurality of wirings respectively connected to said plurality of conductors;

a plurality of blind through holes (BTHs) respectively connected to said plurality of wirings; and

a lead for plating said plurality of conductors, said lead forming an intermediate layer of said laminate printed circuit board located below said plated conductors, connected to said plurality of BTHs, and extending in a direction different from said first direction;

wherein said lead is severed between nearby ones of said plurality of BTHs so that said nearby BTHs are not interconnected through said lead; and

wherein said plurality of conductors are disposed on a common surface of said printed circuit board, wherein the edge of said printed circuit board comprises a first edge, wherein said lead extends toward a second edge of said printed circuit board, and wherein said board has a plurality of holes formed therein, each hole being formed between respective adjacent ones of said plurality of BTHs and extending through said lead so that said adjacent ones of said plurality of BTHs are not interconnected through said lead.

² The Appendix incorrectly reproduces "BTHs" in claim 4 as "BTH's."

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The Examiner relies on the following reference:

Yasuda et al. (Yasuda) 5,347,712 September 20, 1994

Claims 4 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yasuda.

We refer to the final rejection (Paper No. 12) (pages referred to as "FR__"), the examiner's answer (Paper No. 23) (unnumbered pages have been numbered and are referred to as "EA__"), and the communication (Paper No. 26) (noting entry of the reply brief and clarifying the examiner's answer) for a statement of the Examiner's rejection, and to the brief (Paper No. 22) (pages referred to as "Br__") and the reply brief (Paper No. 25) for a statement of Appellant's arguments thereagainst.

OPINION

Grouping of claims

The Examiner's conclusion that claims 4 and 8 stand or fall together (EA2) is erroneous. Appellant's statement that "[w]ith respect to the first (and only) issue on appeal, claims 4 and 8 are considered as a single group" (Br7), is a little confusing because we normally consider a group to be a group of claims that stand or fall together. Nevertheless, Appellant states that claims 4 and 8 do not stand or fall together (Br7) and provides arguments for their separate patentability in the argument section. Accordingly, claims 4 and 8 are addressed separately.

Claim interpretation

Claims 4 and 8 are interpreted to be product-by-process claims because they contain at least one process step, the step of forming a hole to sever the lead between BTHs or conductors. The Examiner previously rejected claims 4 and 8 as indefinite under 35 U.S.C. § 112, second paragraph, as indefinite because claim 4 first recites the leads connected to the plurality of BTHs and then recites the nearby BTHs are

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not connected, and because claim 8 first recites the lead is connected to a plurality of conductors and then recites that nearby connectors are not connected through the lead (FR2).

It is not clear why the rejection was withdrawn.

Nevertheless, the claim language is explained by the product-by-process interpretation. In claim 4, corresponding to Figs. 3A-3C, initially a plurality of BTHs are connected by a lead which is used for plating (Fig. 3A), then holes are formed to sever the lead between BTHs (Figs. 3B & 3C).

Claim 4

We summarize the Examiner's rejection, as best understood, with respect to Fig. 6 of Yasuda as marked up by the Examiner in Appendix B (there is no Appendix A) attached to the examiner's answer. The portion of conductor layer 46 to the left of blind hole 48 is a "conductor[]" provided on said laminate printed circuit board . . . extending in a first direction and toward an edge of said printed circuit board." The conductor is "plated" as shown by plating layer 49 (col. 11, lines 23-26). The portion of conductor layer 46 to the right of blind hole 48 is "wiring[]" respectively connected

to said . . . conductor[]." The blind hole 48 a "blind through hole[] (BTH[]) respectively connected to said . . . wiring[]" by the plating layer 49. The conductor layer 34 is a "lead," "said lead forming an intermediate layer of said laminate printed circuit board located below said plated conductors, connected to said . . . BTH[], and extending in a direction different from said first direction, . . . wherein said lead extends toward a second edge of the printed circuit board," because it can be seen that the conductor layer 34 must extend in a direction in and out of the plane of the paper in order to connect to anything.

The Examiner states (FR4-5; EA3):

Yasuda discloses the claimed invention except multiple ones of the conductor, BTH, wirings and the holes, because he does not show the entire board. It would have been obvious to one of ordinary skill in the art, a[t] the time the invention was made, to repeat the pattern shown in figure 6 of Yasuda to make a complete board, thereby yielding a plurality of conductors, holes, BTHs and wirings, because repeating a known pattern on a circuit board for increased capacity is [sic, was] well known in the electrical arts.

We think what the Examiner intended is that the arrangement of Fig. 6 shows one plated conductor/wiring/BTH pattern, which is equivalent to a cross-section along the axis of one of the terminals 21 and BTHs 10 in Appellant's Fig. 3A.

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Presumably, the Examiner considers that the conductor layer 46 has a limited width in a direction out of the plane of the paper, and that it would have been obvious to repeat this pattern in planes parallel to and spaced from the plane of the paper, with the BTHs aligned along a lead (conductor layer 34) extending out of the plane of the paper. This is the only logical way to get the arrangement of Appellant's Fig. 3. We do not think the Examiner proposes to repeat the pattern to the left or right as shown in Appellant's Appendix D, because this does not result in a plurality of conductors for the reasons argued by Appellant at Br12. Unfortunately, the Examiner's failure to question Appellant's interpretation leaves confusion as to what the Examiner meant.

We assume, for the sake of argument, that it would have been obvious to repeat the pattern in Fig. 6 in planes parallel to and spaced from the plane of the paper so as to create a plurality of plated conductor/wiring/BTHs. (This modification appears to be based solely on hindsight in view of Appellant's disclosure, rather than any identified suggestion in Yasuda or the knowledge of one of ordinary skill in the art, but we assume the Examiner is correct for the

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purposes of this discussion.) The Examiner's modifications would result in the structure at the top half of Appellant's Fig. 3A, i.e., the top set of terminals 21, upper BTHs 10, and (lead) wiring 13 interconnecting the BTHs 10.

The issue is whether the following limitations of claim 4 are taught or suggested by Yasuda: "wherein said lead is severed between nearby ones of said plurality of BTHs so that said nearby BTHs are not interconnected through said lead; . . . and wherein said board has a plurality of holes formed therein, each hole being formed between respective adjacent ones of said plurality of BTHs and extending through said lead so that said adjacent ones of said plurality of BTHs are not interconnected through said lead." These limitations refer to the holes 14 in Fig. 3B and 3C. Appellant argues that these limitations are not disclosed or suggested by Yasuda (Br15-16).

The Examiner states (EA7):

Appellant also argues that the hole does not pass through the lead. Examiner notes that this is not a claim limitation. Therefore, the argument is moot. The claim states that the lead is connected to the hole (it is as seen from figure 6 of Yasuda in appendix B [to the examiner's answer]) and is severed between adjacent holes so that the holes are not connected through the lead (see claim language, for example at lines 12-13 of claim 4).

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Obviously, this is the case: the lead is severed between the holes thereby not connecting them, because it only extend[s] a short distance to either side of each hole as clearly illustrated in appendix B [to the examiner's answer].

Also, the blind through hole (50) is not what is labeled as the BTH in the rejection, see appendix B [to the examiner's answer]. Second, as seen even from appellant's appendix D, the lead does not connect the two BTH's [sic] shown in this figure. Sections of the lead are connected to their respective BTH only in the immediate vicinity of that BTH and completely disconnected from the other BTH.

We do not understand the Examiner's reasoning. According to the Examiner's rejection, the conductor layer 34 in Fig. 6, corresponding to the claimed "lead for plating . . . connected to said plurality of BTHs," extends out of the plane of the paper and connects to a plurality of BTHs. The conductor layer 34 must be physically (and electrically) continuous from one BTH to the next in order to meet the limitation of being "connected to said plurality of BTHs" and to be capable of performing the intended use "for plating." The Examiner cannot dismiss the limitation "for plating" as a statement of intended use which is capable of being performed by conductor layer 34 in Fig. 6 and, at the same time, take the inconsistent interpretation that the conductor layer 34 is severed between BTHs which would make the layer incapable of

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being used "for plating." Yasuda says nothing that would have suggested the Examiner's proposed modification of providing a plurality of plated conductors/wirings/BTHs, where the BTHs are interconnected by a lead extending a different direction than the conductors, and certainly does not disclose or suggest further modifying the Examiner's modification to sever the lead (conductor layer 34 in the rejection) between BTHs. The Examiner's statement that the lead is shown as severed between holes in Yasuda because it only extends a short distance to either side of the hole is not consistent with the Examiner's rejection where the BTHs are arrayed along a lead (conductor layer 34) out of the plane of the paper. Figure 6 only shows the width of the lead (conductor layer 34); it does not show the lead severed between BTHs which were connected at one time for the purpose of plating.

Contrary to the Examiner's statement that the hole passing through the lead is not a claim limitation, claim 4 expressly recites "each hole . . . extending through said lead so that said adjacent ones of said plurality of BTHs are not interconnected through said lead." The Examiner erred in dismissing arguments to this limitation as moot.

The Examiner has failed to establish the obviousness of the limitations "wherein said lead is severed between nearby ones of said plurality of BTHs so that said nearby BTHs are not interconnected through said lead; . . . and wherein said board has a plurality of holes formed therein, each hole being formed between respective adjacent ones of said plurality of BTHs and extending through said lead so that said adjacent ones of said plurality of BTHs are not interconnected through said lead." Accordingly, we conclude that the Examiner has failed to establish a prima facie case of obviousness as to claim 4. The rejection of claim 4 is, therefore, reversed.

Claim 8

The issue involved in claim 8 is similar to that discussed in claim 4. Claim 8 is directed to the embodiment of Figs. 4A and 4B where the lead 22 is connected to a plurality of conductors 21 sideways on the surface of the laminate, i.e., without the intermediate BTHs of the Fig. 3 embodiment. Then the lead is severed between conductors by holes 23 (Fig. 4B).

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The Examiner again fails to show a lead that is used for plating (or capable of being used for plating) a plurality of conductors that is then severed by holes which disconnect the plurality of conductors. We conclude that the Examiner has failed to establish a prima facie case of obviousness as to claim 8. The rejection of claim 8 is, therefore, reversed.

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CONCLUSION

The rejection of claims 4 and 8 is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
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Administrative Patent Judge)	AND
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