

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 44

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ALAN G. WOOD,
EUGENE H. CLOUD,
and
LARRY D. KINSMAN

Appeal No. 2000-0622
Application No. 08/650,894

ON BRIEF

Before HAIRSTON, BARRETT, and GROSS, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 82 through 91, 94 through 96 and 100 through 103. After the submission of the brief, the examiner allowed claims 94 through 96 and 100 through 103 (answer, page 6). Accordingly, claims 82 through 91 remain before us on appeal.

Appeal No. 2000-0622
Application No. 08/650,894

The disclosed invention relates to a method for fabricating a multi-chip module. In the fabrication method, a plurality of semiconductor packages are tested prior to retaining and sealing the packages within a housing.

Claim 82 is the only independent claim on appeal, and it reads as follows:

82. A method for fabricating a multi-chip-module comprising:

a) providing a plurality of semiconductor packages, each package comprising a plurality of package leads and a semiconductor die;

b) testing the packages, by performing functionality testing, adherence to required specifications testing, and burn-in testing;

c) providing a housing for retaining the packages comprising a plurality of conductive traces and a plurality of external leads in electrical communication with the traces;

d) placing passing packages from the testing step within the housing and electrically coupling the passing packages and the conductive traces; and

e) sealing the passing packages within the housing.

The references relied on by the examiner are:

Falanga	4,746,583	May 24, 1988
Ahn et al. (Ahn)	H606	Mar. 7, 1989
Sugano et al. (Sugano)	5,028,986	Jul. 2, 1991

Appeal No. 2000-0622
Application No. 08/650,894

Claims 82 through 84, 87, 88 and 91 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugano in view of Falanga.

Claims 85 and 86 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugano in view of Falanga and well-known prior art.

Claims 89 and 90 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugano in view of Falanga and Ahn.

Reference is made to the brief (paper number 42) and the answer (paper number 43) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 82 through 91.

Appellants and the examiner disagree as to whether Sugano performs tests on the tape mounted chips prior to packaging and sealing them on a connector housing. According to the examiner (answer, page 6), "Sugano is explicitly and clearly shown to teach a process comprising functionality and burn-in testing of semiconductor packages prior to sealing in a housing."

Appeal No. 2000-0622
Application No. 08/650,894

Appellants argue (brief, page 12) that:

In Sugano et al., the TAB packages, which comprise the resin coated chips 1a and the carrier tape 2a, are tested following soldering to the connectors 9a. On the other hand, the presently claimed method tests the packages prior to placing, electrically coupling, and then sealing the packages within the housing. With the present method, if the packages are defective, the costs associated with electrically coupling and sealing the packages within the housing can be eliminated. With Sugano et al. "the defectives can be eliminated before the stacking" (column 23, lines 31-32). However, defective packages can still be soldered to the connectors 9a.

Based upon the teachings of Sugano, we agree with appellants' argument that Sugano does not perform tests on the tape mounted chips prior to packaging and sealing them on the connector housing. Sugano clearly discloses (column 23, lines 11 through 32; Figure 57) that the testing is performed after the tape mounted chips are mounted on the connector housing. Since the sealed housing teachings of Falanga do not cure the noted shortcoming in the teachings of Sugano, the obviousness rejection of claims 82 through 84, 87, 88 and 91 is reversed. The obviousness rejections of claims 85, 86, 89 and 90 are likewise reversed because Falanga, the well-known prior art and the conductive epoxy teachings of Ahn do not cure the noted shortcoming in the teachings of Sugano.

Appeal No. 2000-0622
Application No. 08/650,894

DECISION

The decision of the examiner rejecting claims 82 through 91 under 35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
)	
)	
ANITA PELLMAN GROSS)	
Administrative Patent Judge)	

KWH:hh

Appeal No. 2000-0622
Application No. 08/650,894

STEPHEN A. GRATTON
2764 SOUTH BRAUN WAY
LAKEWOOD, CO 80228