

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AKIHIRO NAKAMURA and YUTAKA HAYASHI

Appeal No. 2000-0660
Application No. 08/985,278

ON BRIEF

Before FLEMING, RUGGIERO, and LALL, ***Administrative Patent Judges.***
FLEMING, ***Administrative Patent Judge.***

Decision on Appeal

This is a decision on appeal from the final rejection of claims 1 through 3 and 5 through 11. Claim 4 has been cancelled.

The invention relates to a nonvolatile one-transistor memory cell. The transistor memory cell includes a channel forming region (11a), a tunnel film (12) formed over the channel forming region (11a), a nitride film (13a) formed over the tunnel film (12), a top oxide (13b) formed over the nitride film (13a) and a gate electrode (14) formed over the top oxide film (13b). See Appellants' specification page 4, line 20 to page 5, line 3, page 10, lines 7-22 and Figure 1. The tunnel film (12) is formed to

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have a thickness of 2.2 nm or more (see Appellants' specification page 10, lines 19-23) and desirably a 3.4 nm or more thickness. See Appellants' specification page 11, lines 6 and 7.

Alternatively, the top oxide (13b) set to almost the same thickness as the thickness of the tunnel film (12) or preferably, the top oxide is set to a smaller thickness than the thickness of the tunnel film wherein the amount of transition of the carriers passing through the top oxide film is almost equal to or larger than the amount of the transition of the carrier passing through the tunnel film. See Appellants' specification page 6, line 22 to page 7, line 6.

Independent claims 1 and 5 and dependent claim 3 are reproduced as follows:

1. A nonvolatile one-transistor memory cell comprising:
 - a channel-forming region of a semiconductor;
 - a tunnel film on said channel forming region;
 - an insulation film on said tunnel film; and
 - a gate electrode on said insulation film,

wherein said insulation film includes a nitride film and a top oxide film on said nitride film, the thickness of the tunnel film being within a range where charges in the channel forming region directly tunnel through the tunnel film and is 2.2 nm or more.

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3. A nonvolatile one-transistor memory cell as set forth in claim 2, wherein the thickness of the tunnel film is 3.4 nm or more.

5. A nonvolatile one-transistor memory cell comprising;
a channel-forming region of a semiconductor;
a tunnel film on said channel forming region;
an insulating film on said tunnel film; and
a gate electrode on said insulation film,

wherein said insulation film comprising a nitride film and a top oxide film on said nitride film, the thickness of said top oxide film being set to a thickness so that the amount of transition of the carriers passing through the top oxide film is almost equal to or larger than the amount of transition of the carriers passing through the tunnel film under a read voltage applied to said gate electrode.

References

The references relied on by the Examiner are as follows:

Hayashi et al. (Hayashi)	4,868,632	Sep. 19, 1989
Hayabuchi	5,324,675	Jun. 28, 1994
Young	5,621,683	Apr. 15, 1997
		(filed Dec. 5, 1995)

Rejections at Issue

Claims 1 and 2 stand rejected under 35 U.S.C. § 102 as being anticipated by Hayashi. Claims 5 and 6 stand rejected under 35 U.S.C. § 102 as being anticipated by Hayabuchi. Claim 3 stands rejected under 35 U.S.C. § 103 as being unpatentable over

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Hayashi and Young. Claims 7 and 9 through 11 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hayashi and Hayabuchi. Claim 8 stands rejected under 35 U.S.C. § 103 as being unpatentable over Hayashi, Hayabuchi and Young.

Rather than repeat the arguments of the Appellants or the Examiner, we make reference to the Reply Brief¹ and the Answer for the respective details thereof.

OPINION

After a careful review of the evidence before us, we agree with the Examiner that claims 1 and 2 are properly rejected under 35 U.S.C. § 102. Thus we will sustain the rejection of these claims but we will reverse the rejection of the remaining claims, claims 3 and 5 through 11, on appeal for the reasons set forth *infra*.

First, we will consider the rejection of claims 1 and 2 under 35 U.S.C. § 102 as being anticipated by Hayashi. We find on page 6, lines 15-19 of the brief, that Appellants have provided a statement that claims 1 and 2 stand and fall together, claims 5, 6, 7, 9 and 10 stand and fall together, and claims 3, 8

¹ Appellants filed an appeal brief, on August 4, 1999. Appellants filed a reply brief on December 9, 1999. The Examiner mailed an office communication on January 13, 2000, stating that the reply brief has been entered.

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and 11 stand or fall together. 37 CFR § 1.192 (c)(7) (July 1, 1999) **as amended at** 62 Fed. Reg. 53196 (October 10, 1997), which was controlling at the time of Appellants' filing the brief, states:

For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

We further note that in the reply brief, Appellants have argued claims 1 and 2 as a single group. See the entire page 11 of the reply brief. We will, thereby, consider Appellants' claims 1 and 2 as standing or falling together as a group and we will treat claim 1 as a representative claim of that group.

Appellants state that "[c]laim 1 recites a 'non-volatile one-transistor memory cell.'" See page 11, lines 2 and 3 of the reply brief. Appellants then argue that the Hayashi transistor would need a second transistor to prevent leakage current. See page 11, lines 7-10 of the reply brief. However, Appellants do

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not disagree that Hayashi teaches all the other claim limitations.

We find that Hayashi et al. clearly teaches that an 'MONOS' type nonvolatile semiconductor memory . . . forms a single transistor memory cell. Therefore, we find that Hayashi teaches a "non-volatile one transistor memory cell" as claimed.

In regard to Appellants' argument as to the leakage current, we find nothing in Appellants' claim limitations that requires the "non-volatile one transistor memory cell" to operate without the leakage current and thereby Appellants' claim language does not preclude the reading of the Hayashi non-volatile one transistor memory cell on Appellants' claim 1.

Appellants have not made any other arguments in regard to the Hayashi reference and claim 1. We therefore find that the teachings of Hayashi meet Appellants' claimed limitation.

Appellant has not made any other arguments. 37 CFR § 1.192 (a) states:

Appellant must, within two months from the date of the notice of appeal under § 1.191 or within the time allowed for reply to the action from which the appeal was taken, if such time is later, file a brief in triplicate. The brief must be accompanied by the fee set forth in § 1.17 (c) and must set forth the authorities and arguments on which appellant will rely to maintain the appeal. Any arguments or authorities not included in the brief will be refused consideration

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by the Board of Patent Appeals and Interferences,
unless good cause is shown.

Thus, 37 CFR § 1.192 provides that only the arguments made by Appellant in the brief will be considered and that failure to make an argument constitutes a waiver on that particular point. Support for this rule has been demonstrated by our reviewing court in *In re Berger*, No. 01-1129, Slip Opinion (Fed. Cir. 2002), wherein the Federal Circuit Court stated that because the Appellant did not contest the merits of the rejections in his brief to the Federal Circuit court, the issue is waived.

We have carefully considered the objective evidence as well as the prior art relied upon by the Examiner. We find that Appellants' claim 1 is properly rejected under 35 U.S.C. § 102. In view of the foregoing, we will sustain the decision of the Examiner rejecting claims 1 and 2 under 35 U.S.C. § 102.

Now we turn to the rejection of claims 5 and 6 under 35 U.S.C. § 102 as being anticipated by Hayabuchi.

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. **See *In re King***, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and ***Lindermann Mashinenfabrik GMBH v.***

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American Hoist & Derrick Co., 730 F.2d 1452, 1458, 221 USPQ 481,
485 (Fed. Cir. 1984).

Appellants' claim 5 recites the following:

wherein said insulation film comprising a nitride film and top oxide film on said nitride film, the thickness of said top oxide film being set to a thickness so that the amount of transition of the carriers passing through the top oxide film is almost equal to or larger than the amount of transition of the carriers passing through the tunnel film under a read voltage applied to said gate electrode.

Appellants argues that "Hayabuchi teaches a tunnel film (3) that is 2 nm thick (col. 3, lines 55-56) and a top oxide layer (5) which is 4 nm thick (col. 3, lines 67-68). Consequently, the 4 nm top oxide layer taught by Hayabuchi cannot pass charge carriers in equal or greater quantity than the thinner 2 nm tunnel film as recited in claim 5." See page 8, lines 25-30 of the reply brief.

On page 4, lines 1-4 of the answer, the Examiner argues that Hayabuchi discloses the nonvolatile semiconductor memory with

a tunnel film (3) having a thickness of approximately 2 nm formed on the channel forming region; an insulating film formed on the tunnel film, the insulating film including a silicon nitride layer (4) and a top oxide layer (5) with a thickness approximately 1 nm; [and] a gate electrode (9) formed on the insulating film.

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The Examiner further argues that

Hayabuchi does not explicitly teach that the thickness of the top oxide being set so that an amount of transition of the carriers passing through the top oxide layer is almost equal to or larger than the amount of transition of the carriers passing through the tunnel film in a read operation. However, in Hayabuchi's device the thickness of the top oxide layer being smaller than the thickness of the tunnel film . . . Hayabuchi's device inherently has the characteristics as claimed.

See page 4, lines 6-9, 13 and 14 of the answer.

"Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention." **RCA Corp. v. Applied Digital Data Sys., Inc.**, 730 F.2d 1440, 1444 221 USPQ 385, 388 (Fed. Cir.), cert. dismissed, 468 U.S. 1228 (1984), citing **Kalman v. Kimberly-Clark Corp.**, 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983). The prior art disclosure need not be expressed in order to anticipate. **Standard Havens Prods., Inc. v. Gencor Indus., Inc.**, 953 F.2d 1360, 1369, 21 USPQ2d 1321, 1328 (Fed. Cir.) **cert. denied**, 506 U.S. 817 (1992).

Furthermore, "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by person of ordinary skill.'" **In**

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re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950 (Fed. Cir. 1999) *citing* **Continental Can Co. v. Monsanto Co.**, 948 F.3d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result for a given set of circumstances is not sufficient." *Id. citing* **Continental Can Co. v. Monsanto, Co.**, 948 F.3d 1264, 1269, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).

Upon careful review of Hayabuchi, we fail to find that Hayabuchi teaches:

. . . said insulation film comprising a nitride film and top oxide film on said nitride film, the thickness of said top oxide film being set to a thickness so that the amount of transition of the carriers passing through the top oxide film is almost equal to or larger than the amount of transition of the carriers passing through the tunnel film under a read voltage applied to said gate electrode,

as recited in Appellants' claim 5. Rather, we find that Hayabuchi forms a second oxide layer 5 (i.e. the top oxide layer) having a thickness of approximately 4 nm over the silicon nitride layer 4. See column 3, lines 65-68. Further, a silicon layer 6 is formed over layer 5 and a resist 8 is formed on layer 6. Then the silicon layer 6 is completely etched away and approximately 1 nm or more of the second oxide layer 5 may remain. See column 4,

lines 1-22 and Figures 1 and 2. However, though we find that as the Examiner states, the oxide layer 5 has a thickness of about 1 nm, this is only true of the areas "not" under the gate 9. See column 4, lines 38-56 and Figure 2. Rather, we find that the top oxide layer 5, under the gate 9, would remain at about 4 nm, which is a greater thickness than the tunnel layer 3 which is about 2 nm. We therefore cannot agree with the Examiner that the Hayabuchi reference teaches the tunnel film (3) having a thickness of approximately 2 nm and a top oxide layer (5) with a thickness approximately 1 nm wherein it is inherent that the thickness of the top oxide is set so that an amount of transition of the carriers passing through the top oxide layer is almost equal to or larger than the amount of transition of the carriers passing through the tunnel film in a read operation. Therefore, we find that Hayabuchi fails to teach all the claim limitations of claim 5 and thereby claim 5 is not anticipated by Hayabuchi.

Further, since we find that claims 6 through 8 are dependent on claim 5, and thereby recite the above limitation of claim 5, we will not sustain the Examiner's rejection of claims 6 through 8 under 35 U.S.C. § 103.

On page 5 lines 14-15 of the answer, the Examiner argues, that independent claim 9 and dependent claims 10 and 11, are

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rejected under 35 U.S.C. § 103 as being unpatentable over Hayabuchi and Hayashi. For the same reasons above with regards to claim 5, we fail to find that the Examiner has shown that Hayabuchi teaches or suggests the above claim 9 limitations. Because claims 10 and 11 depend from claim 9, and therefore include all the limitations of claim 9, we will not sustain the Examiner's rejection of claims 9 through 11 under 35 U.S.C. § 103.

Now we turn to the rejection of claim 3 under 35 U.S.C. § 103 as being unpatentable over Hayashi and Young. We agree with the Examiner's contention that Hayashi teaches the limitations found in claims 1 and 2 but fails to teach that the thickness of the tunnel film being 3.4 nm or more. See page 5, lines 1-4 of the answer. However, the Examiner asserts that "Young discloses a nonvolatile semiconductor memory device comprising a tunnel film (23) having a thickness of 5 nm. See Fig. 2." See page 5, lines 5 and 6 of the answer. The Examiner further states that "[i]t would have been obvious to one of ordinary skill in the art to form the tunnel film with a thickness of 3.4 nm as taught by Young . . . depending on the size of the transistor which is depending on each application" and "[t]he thickness differences are considered obvious design

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choices . . . [and it] appears that these changes produce no functional differences and therefore would have been obvious." See page 5, lines 7-12 of the answer.

Appellants argue that "the thickness of the tunnel film has a very significant, unobvious functional effect . . . [wherein] the thickness (T) of the tunnel directly effects the length of time that the data is retained in the memory transistor." See page 5, line 23 through page 6, line 3 of the reply brief. Further, the Appellants argue that the data retention time "increase continues until the thickness of the tunnel film reaches approximately 3.5 nm. At this point, the data retention time reaches a plateau. (See Fig 2.)" See page 6, lines 5-8 of the reply brief. Lastly, the Appellants argue that "the Examiner has failed to provide any motivation other than the bald allegation of 'mere design choice' to explain why one of skill in the art would have combined the unnecessarily thick tunnel film taught by Young with the memory device taught by Hayashi." See page 6, line 22 through page 7, line 1 of the reply brief.

The Federal Circuit states that, "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch,***

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972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), citing *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). In addition, our reviewing court stated in *In re Lee*, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002), that when making an obviousness rejection based on combination, "there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by Applicant" (quoting *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998)).

We agree with the Appellants that the Examiner has failed to point to any teachings in Young that would suggest the combination of the Young and Hayashi references to achieve the claim 3 limitations. As such, we cannot sustain the Examiner's rejection of claim 3 as being unpatentable under 35 U.S.C. § 103 in view of Hayashi and Young.

In view of the foregoing, the decision of the Examiner rejecting claims 1 and 2 under 35 U.S.C. § 102 is affirmed; however, the decision of the Examiner rejecting claims 5 and 6 under 35 U.S.C. § 102 and rejecting claims 3 and 7 through 11 under 35 U.S.C. § 103 is reversed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

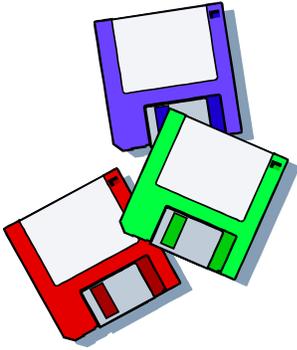
AFFIRMED-IN-PART

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DECISION: AFFIRMED-IN-PART

Prepared: June 5, 2003

Draft Final

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