The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte RICHARD A. KELLEY, DANNY M. NEAL, MICHAEL A. PEREZ, PAUL G. ROBERTSON, PADMAVATHY TAMIRISA and JOHN D. UPTON

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Appeal No. 2000-1187
Application No. 08/723,174

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ON BRIEF

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Before HAIRSTON, JERRY SMITH, and SAADAT, Administrative Patent Judges.

SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1, 5, 6, 10, 11 and 15 through 17.[1]

[1] The rejection of claims 2 through 4, 7 through 9 and 12 through 14 was withdrawn in the answer.

We reverse.

BACKGROUND

The appellants' invention is generally directed to peripheral component interconnect (PCI) systems and in particular, to selection of peripheral devices attached to the system via expansion slots provided by PCI-PCI bridges. Each device is selected using address data lines connected to the input/output of a bus bridge while each data line is connected to a pin of a pin out grid array in each of the expansion slots. The ID select of each device is connected to a pin corresponding to one of the address data lines (specification, p. 6). Alternatively, a logic gate is located between a bridge and an expansion slot with its inputs connected to address data line 0 and the one to which the ID select of the device is connected. The output of a logic gate provides the ID select of the target device (specification, p. 8).

Representative independent claims 1 and 5 are reproduced as follow:

1. An apparatus for selecting a device when said device is a target of a configuration query comprising:

at least a bus bridge having a slot for attaching a device; and

at least a logic gate connected between said bridge and said slot for selecting said device when said device is a true target of said configuration query.

5. An apparatus for selecting a device when said device is a target of a configuration query comprising:

at least a bus bridge having a slot for attaching a device, said bus bridge driving 32 address data lines wherein one of said 32 address data lines is used to enable said device only when said device is a target of said configuration query, said one of said 32 address data lines being a data line reserved to indicate a selected bus.

The prior art reference of record relied upon by the examiner in rejecting the appealed claims is:

Cohen et al. (Cohen) 5,737,524 Apr. 7, 1998

Claims 1, 5, 6, 10, 11 and 15 through 17 stand rejected under 35 U.S.C. § 102 as being unpatentable over Cohen.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted

rejections, we make reference to the answer (Paper No. 12, mailed June 21, 1999) for the examiner's complete reasoning in support of the rejection, and to the brief (Paper No. 11, filed March 8, 1999) and reply brief (Paper No. 13, filed July 23, 1999) for the appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art reference, and to the respective positions articulated by the appellants and the examiner. As a consequence of our review, we make the determinations which follow.

At the outset, we note that the appellants consider claims 1, 6, 11, 16 and 17[2] as one group and claims 5, 10 and 15 as another group (brief, p. 3). The appellants further provide separate arguments for each group (brief, p. 4). Therefore, we will consider the claims as two groups and will treat claims 1 and 5 as the representative claims of their corresponding groups.

[2] Claims 2 through 4, 7 through 9 and 12 through 14 were originally included in the group before the rejection of these claims was withdrawn in the answer.

With respect to claim 1, the appellants argue that Cohen teaches neither "at least a bus bridge having a slot" nor "at least a logic gate connected between said bridge and said slot." The appellants further point out that Cohen uses programmable configuration registers within a VLSI chip to report to the host processor the device ID and the application code of the card being used (brief, p. 4, reply brief, p. 2).

The examiner responds to the appellants' arguments by referring to the last paragraph of the specification that suggests the use of any other logic gates, boards or driving signal for device ID select (answer, p. 4). The examiner concludes that other sources for selecting the target device such as Cohen's activating a control bit after the "retry mode" is de-activated, anticipates the claims (answer, pp. 4 & 5).

A rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference. In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994), citing In re Spada, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990).

We find that Cohen teaches a computer system having a Peripheral Component Interconnect (PCI) bus where add-in boards are provided with a universal interface module that includes programmable PCI configuration registers (col. 2, lines 32-37). Cohen further specifies that the PCI add-in board is mounted in an expansion slot under the cover of the PCI computer system (col. 4, lines 10-15). Cohen further teaches that the module is a PCI bus interface chip placed on the add-in board which interconnects different types of boards (or devices) to the PCI bus by providing the corresponding configuration logic to be used for identifying and selecting the device. We find that, contrary to the claimed logic gate connected between the bridge and the slot, Cohen's add-in board includes the data transfer logic for selecting the target device and is mounted in <u>a slot which is directly connected to the PCI bus</u>.

In view of the analysis above, we find that the examiner has failed to meet the burden of providing a <u>prima facie</u> case of anticipation. We find no teachings in Cohen related to "a bus bridge having a slot for attaching a device" and "a logic gate connected between said bridge and said slot." Additionally, we disagree with the examiner that alternative embodiments or modifications suggested in the appellants' specification can

remedy the deficiencies of Cohen in a rejection based on anticipation. Accordingly, we reverse the rejection of claims 1, 6, 11, 16 and 17 under 35 U.S.C. § 102 over Cohen.

Turning to the rejection of claims 5, 10 and 15, the appellants argue that Cohen lacks any teachings related to a bus bridge driving 32 address data lines and using one of the 32 address data lines reserved to select local buses for enabling the device. The appellants further point out that the reference fails to anticipate the claims since it does not discuss the subject of address data lines (brief, p. 4).

The examiner, in response, points to col. 2, lines 51-59 of Cohen for teaching the activation of selected control lines on the PCI bus by the PCI interface chip in response to accesses to its registers from the system processor (answer, p. 6). The examiner further refers to the [PCI] control [signal] lines between PCI bus 10 and PCI state machine and combinatorial logic means 31 (Fig. 4) as the address line.

Cohen in col. 6, lines 35 through 43 states:

> Still referring to Fig. 4, <u>a set of the data lines (on the PCI bus) called the PCI data bus 10A</u> interconnects the PCI configuration registers to PCI bus 10. <u>a control architectured line called the PCI-RST#LINE</u> interconnects the PCI access grant register 24 to the PCI bus 10. Finally, <u>a set of PCI control signal lines</u> necessary to activate the so-called retry function of the PCI bus, interconnects the

> PCI [b]us 10 to the PCI Slave State Machine and Combinatorial logic means 31 (emphasis added).

We find that Cohen's data lines (10A) are separate from control lines which are connected between the PCI bus and the access grant register(PCI-RST#LINE) as well as the logic means on the PCI bus interface chip(PCI control signal lines). Additionally, Cohen provides no teachings related to a bus bridge driving 32 address data lines and using one of the 32 lines reserved to select local buses for enabling the device. We disagree with the examiner's characterization of "selected control lines on the PCI bus" as the address data lines since Cohen's control lines are dedicated control lines and are clearly separate from data lines 10A. Therefor, we find that the examiner has not met the burden of providing a prima facie case of anticipation. Accordingly, we reverse the rejection of claims 5, 10 and 15 under 35 U.S.C. § 102 over Cohen.

CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1, 5, 6, 10, 11 and 15 through 17 under 35 U.S.C. § 102 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
JERRY SMITH Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
MAHSHID D. SAADAT Administrative Patent Judge	)	

MDS/ki

Volel Emile
P. O. Box 202170
Austin, TX 78720

MDS/ki