

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 30

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HAJIME INOUE
and
NAOFUMI YANAGIHARA

Appeal No. 2000-1282
Application No. 08/813,140

HEARD: FEBRUARY 21, 2002

Before HAIRSTON, RUGGIERO, and SAADAT, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 46. In an Amendment After Final (paper number 22), claims 1 and 9 were amended.

The disclosed invention relates to a method and apparatus for recording or reproducing digital signals. The digital signal recording and the digital signal reproduction are each

Appeal No. 2000-1282
Application No. 08/813,140

performed in a two-phase operation in first and second portions of a digital memory.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. Apparatus for recording a digital signal and redundancy signals such that said digital signal may be reproduced by error correcting the recorded digital signal using the redundancy signals, comprising

a digital memory,

a digital storage system providing recordation of digital information,

error correcting circuitry receiving a group of digital signals and generating therefrom redundancy signals to be used in error correction of said digital signals, and

control circuitry controlling operations of said memory, said digital storage system and said error correcting circuitry to receive digital signals from a signal source, error-encode and record the error-encoded digital signals, wherein

said control circuitry, in a first phase of a recording operation performed during a first period of time, causes a first error-encoded digital signal in a first portion of said memory to be forwarded to said digital storage system for recordation, and causes digital signals from said signal source to be stored in place of said first error-encoded digital signal, while simultaneously causing said error correcting circuitry to error encode digital signals stored in a second portion of said digital memory to form an error-encoded result and store said error-encoded result into said second portion of said digital memory,

Appeal No. 2000-1282
Application No. 08/813,140

said control circuitry, in a second phase of said recording operation performed during a second period of time, causes a second error-encoded digital signal in the second portion of said memory to be forwarded to said digital storage system for recordation, and causes digital signals from said signal source to be stored in place of

Appeal No. 2000-1282
Application No. 08/813,140

said second error-encoded digital signal, while simultaneously causing said error correcting circuitry to error encode digital signals stored in the first portion of said digital memory to form an error-encoded result and store said error-encoded result into said first portion of said digital memory, and

said control circuitry alternately performs said first and second phases of said recording operation such that said first period of time and said second period of time are nonoverlapping.

The references relied on by the examiner are:

Glover et al. (Glover)	4,564,945	Jan. 14, 1986
Lang	4,963,995	Oct. 16, 1990
Lane et al. (Lane)	5,377,051	Dec. 27, 1994
Denissen et al. (Denissen) EP 0 553 515 A2 (published European Patent Application)		Aug. 4, 1993

Claims 1 through 3, 8 through 12, 25 through 27 and 31 through 34 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Denissen.

Claims 4 through 7, 13 through 22, 28 through 30 and 35 through 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Denissen in view of Lane.

Claims 23 and 45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Denissen in view of Glover.

Claims 24 and 46 stand rejected under 35 U.S.C. § 103(a)

Appeal No. 2000-1282
Application No. 08/813,140

as being unpatentable over Denissen in view of Lang.

Appeal No. 2000-1282
Application No. 08/813,140

Reference is made to the brief (paper number 25) and the answer (paper number 26) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the 35 U.S.C. § 102(b) rejection of claims 1 through 3, 8 through 12, 25 through 27 and 31 through 34, and the 35 U.S.C. § 103(a) rejection of claims 4 through 7, 13 through 24, 28 through 30 and 35 through 46.

To anticipate a claim, a single prior art reference must disclose each and every limitation of the claim. Glaxo Inc. v. Novopharm Ltd., 52 F.3d 1043, 1047, 34 USPQ2d 1565, 1567 (Fed. Cir.), cert. denied, 516 U.S. 3378 (1995).

According to the appellants (brief, page 8), the first and second portions of the claimed digital memory are used as follows:

Thus, in the invention recited in the claims, in a first phase, data stored in the second portion is error encoded/corrected, while in the first portion raw and encoded/corrected data are written and read, respectively. Thus, the second portion is used as a workspace for error encoding/correcting, and the first portion is used as a buffer. In the second phase, data stored in the first portion is error encoded/corrected,

Appeal No. 2000-1282
Application No. 08/813,140

while in the second portion raw and encoded/corrected data are written and read, respectively. Thus, the first portion is used as a workspace for error encoding/correcting, and the second portion is used as a buffer.

Appellants argue (brief, page 9) that "DENISSEN uses his memory only as a buffer," whereas appellants use "a memory both as a workspace for error correcting/encoding, and as a buffer for raw and corrected/encoded data." As a second point of distinction, appellants argue (brief, page 13) that:

[T]he present claims further clearly distinguish DENISSEN in that the present claims recite a memory divided into two portions which are used in an alternating fashion: one portion is used for error correction or error encoding while the other portion is used for storage of new data and output of previously corrected or encoded signals. DENISSEN does not allocate the two halves of his memory 1.12 in such a fashion. DENISSEN allocates space in two halves of memory 1.12 to hold previous or newly-arrived data, based on the results of previous error corrections and previous identification(s) of unreliable data, meaning that at any point in time data is allocated essentially randomly between two half-memories (see Fig. 3C), rather than in an alternating fashion as is recited in the present claims.

We agree with appellants' arguments. Thus, the 35 U.S.C. § 102(b) rejection of claims 1 through 3, 8 through 12, 25 through 27 and 31 through 34 is reversed because the two-sectioned memory 1.12 in Denissen does not operate in an

Appeal No. 2000-1282
Application No. 08/813,140

alternating manner as set forth in the claims on appeal.

Appeal No. 2000-1282
Application No. 08/813,140

The 35 U.S.C. § 103(a) rejection of claims 4 through 7, 13 through 24, 28 through 30 and 35 through 46 is reversed because the teachings of Lane, Glover and Lang do not cure the noted shortcomings in the teachings of Denissen.

DECISION

The decision of the examiner rejecting claims 1 through 3, 8 through 12, 25 through 27 and 31 through 34 under 35 U.S.C. § 102(b) is reversed, and the decision of the examiner rejecting claims 4 through 7, 13 through 24, 28 through 30 and 35 through 46 under 35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
JOSEPH F. RUGGIERO)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
)	
)	
MAHSHID D. SAADAT)	

Appeal No. 2000-1282
Application No. 08/813,140

Administrative Patent Judge)

KWH:hh

Appeal No. 2000-1282
Application No. 08/813,140

THOMAS W. HUMPHREY
WOOD, HERRON AND EVANS
2700 CAREW TOWER
CINCINNATI, OH 45202