

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN KENNETH SEVERN

Appeal No. 2001-0014
Application No. 09/070,899

ON BRIEF

Before BARRETT, FLEMING and SAADAT, ***Administrative Patent Judges.***

SAADAT, ***Administrative Patent Judge.***

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 6 through 8, which are all of the claims pending in this application.

We REVERSE.

BACKGROUND

The appellant's invention relates generally to hermetic enclosures for opto-electronic devices and more specifically, to hermetically packaged photodetector arrays which do not require an hermetic optical fibre/guide feedthrough (specification, p. 2). A rear light-entry planar semiconductor photodiode array chip is processed to form the active regions and patterned to define a set of contact areas (specification, p. 3). Solder coatings cover and conform in shape to corresponding underlying contacts. The photodiode array chip is bonded face down onto a ceramic substrate to provide electrical connection between the contacts on the chip and metallization on the ceramic substrate as well as form the seal for hermetic enclosure (specification, p. 4). Thus, the individual photodiodes of the array may be optically coupled with ends of individual optical fibers through the rear surface of the chip.

Representative independent claim 6 is reproduced as follows:

6. An opto-electronic device array assembly including a semiconductor chip having a monolithic array of planar construction semiconductor opto-electronic rear light entry/exit devices, which chip is bonded with solder face down upon a ceramic substrate so as to constitute an

hermetic enclosure with opposed walls constituted respectively by the chip and the ceramic substrate, and wherein electrical contact with each opto-electronic device of the array is made by way of electrically conductive connections at least one of which includes an electrically conductive via extending through the thickness of the ceramic substrate.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Chen et al. (Chen) 1991	5,041,900	Aug. 20,
VanZeghbroeck 1997	5,600,130	Feb. 4,
Sato et al. (Sato '419) 1998	5,719,414	Feb. 17,
Sato et al. (Sato '566)	5,798,566	Aug. 25, 1998
Edwards et al. (Edwards) 16, 1999	5,881,945	Mar.

(filed Apr. 30, 1997)

Claims 6 and 7 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sato '566 in view of VanZeghbroeck, Chen and Sato '414. Claim 8 stands rejected under 35 U.S.C. § 103 as being unpatentable over Sato '566, VanZeghbroeck, Chen and Sato '414 in combination with Edwards. We note that claims 6 through 8 were also rejected under 35 U.S.C. § 101 and § 112 as set forth in the final rejection (Paper No. 12, mailed December 9, 1999), which were neither included nor argued in the answer. We assume that these other grounds of

rejection have been withdrawn by the examiner since they were not included in the examiner's answer. *See Ex parte Emm*, 118 USPQ 180, 181 (Bd. App. 1957).

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellant regarding the above-noted rejections, we make reference to the answer (Paper No. 26, mailed July 17, 2000) for the examiner's complete reasoning in support of the rejections, and to the brief (Paper No. 25, filed June 13,

2000) and reply brief (Paper No. 27, filed September 12, 2000) for the appellant's arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellant's specification and claims, to the applied prior art references, and to the respective positions articulated by the appellant and the examiner. After careful review of the evidence before us, it is our conclusion that the evidence provided by the examiner

is insufficient to establish a *prima facie* case of obviousness. Accordingly, we will not sustain the examiner's rejection of claims 6 through 8 under 35 U.S.C. § 103. Our reasoning for this determination follows.

Turning to the grouping of the claims, we note that the appellant on page 4 of the brief points out that the claims do not stand or fall together. 37 CFR § 1.192(c)(7) (July 1, 1999) states:

For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

Although the appellant has provided a statement regarding the groupings of the claims, the appellant has not in the argument section of the brief provided separate arguments for claims 6 and 7 and has only supplemented the main arguments with brief discussion of Edwards for claim 8. We will, thereby, consider the appellant's claims 6 through 8 as

standing or falling together as a group and we will treat claim 6 as the representative claim of that group.

The appellant argues that the applied references do not teach or suggest the recited features related to a chip that is bonded face down upon a ceramic substrate so as to hermetically seal the enclosure formed by the chip and the substrate. In particular, the appellant asserts that hermetically sealing of an electrical feedthrough between the substrate and a chip, as disclosed by Chen, requires high temperature bonding that would severely degrade the diode junctions in the claimed structure due to unwanted diffusion (brief, p. 7). Furthermore, the appellant argues that the insulating bonding layer of Chen results in a seal that itself is electrically insulating and houses feedthroughs whereas the hermetic seal of the claimed invention is made of electrically conductive solder and cannot house

feedthroughs (brief, p. 8). The appellant concludes that, absent appellant's own disclosure, there are no reasons for combining teachings from different references to arrive at the appellant's invention that removes the need for a separate

container by using the chip itself to form one of the walls in a hermetic enclosure.

In response to the appellant's arguments, the examiner states that Chen is relied upon for showing chip-to-substrate bonding to produce an hermetic seal and VanZeghbroeck is relied on to teach solder bonding (answer, p. 5). The examiner points out that the relationship between the seal and the electrical connection to the outside of the package is not relevant to Chen. The examiner further argues that the reason for combining the noted teachings from each reference is based on known techniques that desire hermetically sealing of devices from environmental effects (answer, p. 6).

As pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is the claim." *In re Hiniker Co.*, 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998). Claims will be given their broadest reasonable interpretation consistent with the specification, and limitation appearing in the specification are not to be read into

the claims. ***In re Etter***, 756 F.2d 852, 858, 225 USPQ 1, 5
(Fed. Cir. 1985).

We note that Appellant's claim 6 recites

... which chip is bonded with solder face down upon a ceramic substrate so as to constitute an hermetic enclosure with opposed walls constituted respectively by the chip and the ceramic substrate, and wherein electrical contact with each opto-electronic device of the array is made by way of electrically conductive connections at least one of which includes an electrically conductive via extending through the thickness of the ceramic substrate.

We find that the claim under appeal requires that the device side of the chip be bonded with conductive solder to the ceramic substrate. The claim further requires that contact to each device in the array be made by at least a conductive via extending through the thickness of the substrate and the conductive solder contacting each device. We note that the same solder forms the hermetic seal for an enclosure constituted by the chip and the substrate.

In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a ***prima facie*** case of obviousness. ***See In re Rijckaert***, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). A ***prima facie*** case of obviousness is established by presenting evidence that the

reference teachings would appear to be sufficient for one of ordinary skill

in the relevant art having the references before him to make the proposed combination or other modification. **See In re Lintner**, 458 F.2d 1013, 1016, 173 USPQ 560, 562 (CCPA 1972). Furthermore, the conclusion that the claimed subject matter is **prima facie** obvious must be supported by evidence, as shown by some objective teaching in the prior art or by knowledge generally available to one of ordinary skill in the art that would have led that individual to combine the relevant teachings of the references to arrive at the claimed invention. **See In re Fine**, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

The examiner has failed to set forth a **prima facie** case of obviousness. We disagree with the examiner that the chip-to-substrate bonding of Chen in combination with the teachings of Sato '566 and '414 and VanZeghbroeck would result in the claimed hermetically sealed opto-electronic device or its advantages were known to one of ordinary skill in the art. In

that regard, while Sato '566 discloses a ceramic substrate with a die attach area and a number of contact pins on one surface of the substrate (Fig. 5A and col. 10, lines 6-24), the reference does not teach or suggest bonding the chip face down with solder upon a ceramic substrate to hermetically seal the chip-substrate enclosure. Furthermore, we do not find contact pins 3 to be extending through the thickness of the ceramic substrate. Figure 17 of Sato '566, at the best, merely discloses conductive vias extending through the thickness of package base 31 while chip 32 is bonded face up to package cap 34 and heat radiating member 35. Additionally, we find that the hermetic sealing of the package is achieved by bonding the perimeter of cap 34 to base 31 not by bonding the chip to the substrate so as to constitute an hermetic enclosure.

VanZeghbroeck discloses an optoelectric detector array and a laser array that are physically and electrically connected to each other with solder bumps forming electrical contacts between the circuitry on the detector array and individual lasers on the laser array (col. 3, lines 60-62). Sato '414 also relates to an optoelectric device including an array of PIN photo diodes. However, we find that neither

VanZeghbroeck nor Sato '414 discloses bonding a chip with solder upon a ceramic substrate and using the active device chip as one of the walls for hermetically sealing the enclosure.

We further find that Chen discloses a method of bonding a silicon chip having a cavity to an insulating glass substrate which hermetically seals the cavity and the conductive feedthrough line formed on the substrate. The bonding requires

field-assisted bonding technique that heats a layer of silicon oxide facing at high temperature while the chip and the substrate are pressed together under application of a voltage (col. 4, lines 34-38). Thus, the feedthrough line of Chen is actually insulated within the facing layer and sandwiched between the chip and the substrate. Furthermore, the device of Chen is a capacitive pressure sensor that includes only a cavity in silicon chip having a thinned down portion and an electrode for converting pressure to electrical signals (col. 3, line 31). Therefore, unlike an array of opto-electronic devices as recited in the appellant's claim 6, no active

region is present on the silicon chip that may require an electrical contact or be damaged by unwanted diffusion during high temperature bonding.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). It is well settled that it is the teachings of the prior art taken as a whole which must provide the motivation or suggestion to combine the references. ***Fritch***,

972 F.2d at 1266, 23 USPQ2d at 1783-84 (Fed. Cir. 1992) and ***Uniroyal, Inc. v. Rudkin-Wiley Corp.***, 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988). As the court in ***Uniroyal***, 837 F.2d at 1051, 5 USPQ2d at 1438 stated, "it is impermissible to use the claims as a frame and the prior art

references as a mosaic to piece together a facsimile of the claimed invention."

Absent the appellant's own disclosure, we can think of no reason why one of ordinary skill in this art would have been motivated to combine the diverse teachings of Sato references and VanZeghbroeck with Chen as the examiner has proposed. Here, the teachings of Sato '566, VanZeghbroeck and Sato '414 are directed to completely disparate types of devices from that of Chen and, in our view, the examiner has impermissibly relied upon the appellant's own disclosure in arriving at a conclusion of obviousness. Sato '566 is concerned with forming a heat sink on the back surface of the ceramic package opposite the die attach area. Sato, at the best, provides hermetically sealed cap and base ceramic portions with a die attach area under the cap portion while the electrical contacts to the chip are made through the base portion. Sato '414 merely teaches a photoelectric conversion device and its processing method. VanZeghbroeck, on the other hand, relates to an opto-electronic

module formed by attaching a detector array to a laser array using solder bumps without any concern for hermetically sealing the module. Finally, Chen provides a method of hermetically sealing an electrical feedthrough line by bonding a semiconductor chip to an insulating substrate in a pressure sensor. Chen, in fact, is concerned with sealing the feedthrough line between the chip and the substrate in an insulating bonding layer and requires neither active devices on the semiconductor chip nor contacts to such devices by electrically conductive vias extending through the thickness of the ceramic substrate. Therefore, we find no reason or suggestion for combining various teachings from these references, as set forth by the examiner, to arrive at the appellant's claimed invention. In our view, the only suggestion for modifying Sato '566 and '414, VanZeghbroeck and Chen in the manner proposed by the examiner to meet the above-noted limitations stems from hindsight knowledge derived from the appellant's own disclosure. As noted above, the use of such hindsight knowledge to support an obviousness rejection under 35 U.S.C. § 103 is, of course, impermissible.

We fail to find any suggestion or teachings to use Chen's sealed feedthrough in combination with Sato '566,

VanZeghbroeck and Sato '414 such that the opto-electronic chip may be bonded

with solder face down on a substrate as recited in the appellant's claim 6. Therefor, we reverse the rejection of claims 6 and 7 under 35 U.S.C. § 103 over Sato '566 and '414, VanZeghbroeck and Chen. Edwards does not cure the above-mentioned deficiencies with respect to the rejection of claim 6. Accordingly, the rejection of claim 8 under 35 U.S.C. § 103 is reversed.

CONCLUSION

In view of the foregoing, the decision of the examiner to reject claims 6 to 8 under 35 U.S.C. § 103 is reversed.

REVERSED

LEE BARRETT)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
MICHAEL R. FLEMING)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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