

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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**Ex parte** FRANK S. JOHNSON

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Appeal No. 2001-0297  
Application No. 09/196,375

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ON BRIEF

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Before KRASS, DIXON, and BLANKENSHIP, **Administrative Patent Judges**.  
DIXON, **Administrative Patent Judge**.

**DECISION ON APPEAL**

This is a decision on appeal from the examiner's final rejection of claims 3-5 and 8-10, which are all of the claims pending in this application.

We REVERSE.

## BACKGROUND

Appellant's invention relates to a bipolar transistor with a high breakdown voltage collector. The transistors are used in combination for both high speed operation and for large drive currents on the same monolithic integrated circuit. An understanding of the invention can be derived from a reading of exemplary claim 3, which is reproduced below.

3. An integrated circuit, comprising:

a first transistor including:

a first doped buried region within a semiconductor body, said first doped buried region including a portion having a first thickness and a portion having a second thickness, said first thickness being less than said second thickness;

a first collector region disposed over said buried region;

a first base region with said collector region; and

a first emitter region within said base region;

said first collector, said first base region and said first emitter region being disposed over said buried region having a first thickness and at least said first emitter region and said first base region extending over said portion having a second thickness; and

a second transistor including:

a second doped buried region with said semiconductor body, said second doped buried region being substantially uniform in thickness;

a second collector region over said second buried region;

a second base region within said second collector region; and

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a second emitter region within said second base region.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Akcasu	4,644,383	Feb. 17, 1987
Maeda et al. (Maeda)	5,014,106	May 07, 1991

Claims 5 and 10 stand rejected under 35 U.S.C. § 112, first paragraph as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. Claims 3-5 and 8-10 stand rejected under 35 U.S.C. § 103 as being unpatentable over Maeda in view of Akcasu.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellant regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 12, mailed Jun. 14, 2000) for the examiner's reasoning in support of the rejections, and to appellant's brief (Paper No. 11, filed Mar. 14, 2000) and reply brief (Paper No. 13, filed Jul. 24, 2000) for appellant's arguments thereagainst.

## OPINION

In reaching our decision in this appeal, we have given careful consideration to appellant's specification and claims, to the applied prior art references, and to the respective positions articulated by appellant and the examiner. As a consequence of our review, we make the determinations which follow.

**35 U.S.C. § 112, FIRST PARAGRAPH**

Appellant argues that the Summary of the Invention at page 4 and the description of Figure 5 at pages 5 and 12 of the specification provide support for claim 5. We disagree with appellant. We find that the cited portions of the specification and Figure 5 do not clearly show whether the first and second transistors were contemplated to be MOS or CMOS transistors as recited in dependent claim 5. Rather, the specification and Figure 5 tend to imply that CMOS or MOS transistors "may also" be included on the integrated circuit in addition to the first and second bipolar transistors, while the last paragraph of the specification states that the described embodiment is not limiting, we find no other teaching or suggestion in the original twelve pages of the specification that the claimed structure can be extended to MOS or CMOS transistors. With this said, we cannot sustain the rejection of claims 5 and 10 under a lack of written description rejection. From our review of the application at the time of filing, we have found that subject matter of dependent claim 5 was originally filed with the application and its parent claim 3 had similar limitations to present claim 3. Therefore, appellant had possession of the claimed subject matter at the time of filing of

the application. Accordingly, even though we completely agree with the examiner's analysis, we cannot sustain the rejection based upon a lack of written description.

**35 U.S.C. § 103**

Appellant argues that the result of the combined structure of claim 3 is to allow transistors designed for both high  $BV_{ce0}$  and high  $f_t$  to be formed on the same monolithic integrated circuit and in a cost efficient manner without added steps. (See brief at page 4.) Appellant argues that no such structure is taught by Maeda, Akcasu or combination thereof. (See brief at page 4.) Appellant argues that the solution to the problem recognized by the present invention is not taught or suggested. (See brief at page 4.) We disagree with appellant that the combination of Maeda and Akcasu must teach or suggest the same solution that appellant has achieved. Rather, we find the examiner's stated motivation to increase the packing density to be convincing. (See answer at page 6.) Additionally, the examiner maintains that the language of claim 3 does not require transistors designed for both high  $BV_{ce0}$  and high  $f_t$  to be formed on the same monolithic integrated circuit and in a cost efficient manner without added steps. (See answer at page 6.) We agree with the examiner.

With this said, it is the examiner's initial burden to establish a *prima facie* case of obviousness. While we agree with the examiner that the references are properly combinable, we find no motivation to limit the teachings of Akcasu to one of the two transistors taught by Maeda. In our view, Akcasu teaches the use of varied thickness

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for all of the transistors on the integrated circuit to achieve the increased density. While Akcasu teaches the varied thickness for reducing capacitance and increasing density, we find no teaching or suggestion that these benefits may be achieved with one varied thickness transistor and one uniform transistor. Therefore, we find that the examiner has not established that the combination of teachings would have taught or suggested the use of one transistor with a buried region of varied thickness and one transistor with a buried region uniform thickness transistor, and we cannot sustain the rejection of independent claim 3 and its dependent claims 4, 5, and 8-10.

### **CONCLUSION**

To summarize, the decision of the examiner to reject claims 3-5 and 8-10 under 35 U.S.C. § 103 is reversed.

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**REVERSED**

ERROL A. KRASS	)	
Administrative Patent Judge	)	
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	)	
	)	BOARD OF PATENT
JOSEPH L. DIXON	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
	)	
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HOWARD B. BLANKENSHIP	)	
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