

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GUY DUPENLOUP

Appeal No. 2001-0571
Application No. 09/026,790

ON BRIEF

Before THOMAS, GROSS, and LEVY, Administrative Patent Judges.
LEVY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-6 and 9-20, which are all of the claims pending in this application.

BACKGROUND

Appellant's invention relates to automatic synthesis script generation for a synopsis design compiler. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced as follows:

1. A method of generating synthesis scripts to synthesize integrated circuit (IC) designs from a generic netlist description into gate-level description, said method comprising the steps of:

identifying hardware elements in the generic netlist;

determining key pins for each of said identified hardware elements;

extracting design structure and hierarchy from the Generic netlist;

generating script to cause a logic synthesis tool to apply bottom-up synthesis to modules and sub-modules of the IC design;

generating script to cause a logic synthesis tool to apply top-down characterization to modules and sub-modules of the IC design; and

generating script to cause a logic synthesis tool to repeat said bottom-up and said top-down applications until constraints are satisfied.

The prior art reference of record relied upon by the examiner in rejecting the appealed claims is:

Gupte et al (Gupte)	5,812,416	September 22, 1998 (filed July 18, 1996)
---------------------	-----------	---

Claims 1-6 and 9-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Gupte. Rather than reiterate the conflicting viewpoints advanced by the examiner and appellant regarding the above-noted rejection, we make reference to the examiner's answer (Paper No. 11, mailed October 3, 2000) for the examiner's complete reasoning in support of the rejection, and to

appellant's brief (Paper No. 10, filed August 24, 2000) for appellant's arguments thereagainst. Only those arguments actually made by appellant have been considered in this decision. Arguments which appellant could have made but chose not to make in the brief have not been considered. See 37 CFR 1.192(a).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejection advanced by the examiner, and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellant's arguments set forth in the brief along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

Upon consideration of the record before us, we reverse, essentially for the reasons set forth by appellant.

To anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently. In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

Appellant asserts (brief, page 6) that with respect to Group 1 (claims 1-6 and 15) Gupte does not disclose at least the features of "(i) identifying hardware elements in a generic netlist; (ii) determining key pins for each of such identified hardware elements; or (iii) extracting design structure and hierarchy from a generic netlist." With regard to Group 2 (claims 9, 10, 14, and 18-20) appellant asserts (brief, page 9) that "[g]upte does not disclose at least the features of: (i) determining key pins for identified hardware elements from a generic netlist; or (ii) extracting critical design structure and hierarchy from the generic netlist." The examiner's position (answer, page 13) is that appellant's specification (page 2) defines a generic netlist as a netlist created from RTL code that has not yet been correlated with a technology specific library of cells. The examiner argues that when HDL code is not technology specific, it must be considered generic, and that the arbitrary HDL code is synonymous with appellant's definition of a generic netlist. The examiner acknowledges (answer, page 14) that Gupte does not use the term "generic netlist," but asserts that Gupte teaches the elements of a generic netlist when Gupte specifies and illustrates non-technology specific HDL code. The examiner

specifically asserts (answer, page 16) that "Gupte's HDL code is a generic netlist."

From the position taken by the examiner and our review of Gupte, we agree with the examiner that Gupte is silent as to the phrase "generic netlist." Thus, we find that the examiner relies upon inherency to establish anticipation of appellant's claims. As stated in In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981) (quoting Hansgirg v. Kemmer, 102 F.2d 212, 214, 40 USPQ 665, 667 (CCPA 1939)) (internal citations omitted):

Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. If, however, the disclosure is sufficient to show that the natural result flowing from the operation as taught would result in the performance of the questioned function, it seems to be well settled that the disclosure should be regarded as sufficient.

From our review of Gupte, we find no teaching or suggestion of a generic netlist being created and analyzed in Gupte, but rather that in Gupte (col. 13, line 65 through col. 14 ,line 3) the synthesis tool 714 receives as input, HDL code and constraints files 708, and foundry technology libraries 716 to produce gate level netlists 718 (figure 12).

Although we agree with the examiner (answer, page 13) that appellant's specification refers to generic netlists as a netlist that is created from the RTL code that has not yet been correlated with a technology specific library of cells, we agree with appellant (brief, page 3) that synthesis tools typically generate a generic netlist as an intermediate step to producing a final technology-dependent netlist from the input HDL code, and that analysis of the generic netlist will identify many design issues that are missed when only analyzing HDL code. We find support for appellant's assertions in figures 12, 13, and 36, which explain the process for analyzing and elaborating on the input RTL code in HDL format, to produce a generic netlist, remove it from compiler 352 as a dump file, and then analyzing the generic netlist in the process of creating the gate level technology-specific netlist. Although Gupte discloses (col. 4, lines 56-61) that during the design phase, arbitrary HDL code is transformed into Synthesizable Behavioral HDL code, we find no teaching or suggestion in Gupte that arbitrary HDL code is a generic netlist. We are cognizant of the disclosure of Gupte (col. 7, lines 36-39) that an I/O netlist is generated at the chip level at step 218, and that the I/O netlist may be used to simulate the application specific ICs. However, we find no

disclosure or suggestion that the I/O netlist is a generic netlist that is analyzed instead of analyzing the HDL code. Accordingly, we agree with appellant (brief, page 3) that Gupte adaptively generates scripts for driving the synthesis tool based upon the input HDL code. As we stated, supra, inherency cannot be established by possibilities or probabilities, but must naturally flow from the operation of Gupte. Because we find no support for the examiner's assertion that Gupte's HDL code is inherently a generic netlist, we would have to resort to speculation to find support for the examiner's position. The examiner may not resort to speculation or unfounded assumptions to supply deficiencies in establishing a factual basis. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967). From all of the above, we find that the examiner has failed to establish a prima facie case of anticipation of the claimed invention. The rejection of claims 1-6 and 9-20 under 35 U.S.C. § 102(e) is therefore reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1-6 and 9-20 under 35 U.S.C. § 102(e) is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
)	
)	
)	
)	BOARD OF PATENT
ANITA PELLMAN GROSS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
)	
STUART S. LEVY)	
Administrative Patent Judge)	

Appeal No. 2001-0571
Application No. 09/026,790

Page 9

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106 LEGAL
MILPITAS, CA 95035