The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte HERBERT BOLDL

Appeal No. 2001-1352
Application 08/802,828

ON BRIEF

Before THOMAS, DIXON, and BLANKENSHIP, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellant has appealed to the Board from the examiner's final rejection of clams 1-3 and 5-17. Representative claim 1 is reproduced below:

1. A dictation apparatus for storing a speech signal in addressable memory means, the device comprising

- input means for receiving the speech signal,

- data compression means for data compressing the speech signal into a data compressed speech signal, the data compression means being adapted to carry out a data compression step on the speech signal in one of at least two different data compression modes, the at least two different data compression modes resulting in different data compression ratios when applied to the same speech signal, the said at least two different data compression modes being selectable by a user, the data compression means being further adapted to create data files comprising a data compressed speech signal, the data files comprising a header portion, the data compression means being also adapted to generate an identifier signal identifying the data compression mode selected and being adapted to store said identifier signal in said header portion,

- storing means for storing the data files in the memory means, the storing means comprising address generator means for generating addresses for said addressable memory means, for storing blocks of information comprised in a data file in the memory means,

- control means selectively operable by a user for providing an insert signal and an end of insert signal,

- pointing vector generator means for generating a block of pointing vectors in response to the occurrence of each insert signal, said block of pointing vectors comprising a first address signal corresponding to an address of where a dictation insert should be placed in the data file and a second address signal corresponding to a beginning address of an available portion of said addressable memory for storing the dictation insert.

The following references are relied on by the examiner:

Baron	4,053,840	Oct. 11, 1977
Mozer et al. (Mozer)	4,384,170	May 17, 1983
Oye et al. (Oye)	4,791,660	Dec. 13, 1988
Bissonnette et al. (Bissonnette)	5,602,963	Feb. 11, 1997 (filed Oct. 12, 1993)

Microsoft Press Computer Dictionary, Second Edition, pages 294-95 (1994).

All claims on appeal stand rejected under 35 U.S.C. § 103. As to claims 1-3, 5 and 6, the examiner relies upon Bissonnette in view of Mozer or Baron or Oye, with the addition of appellant's admitted prior art and the Computer Dictionary as to claims 7-11. The rejection of dependent claim 12 and the remaining claims 13-17 is questionable. As stated at pages 6-7 of the answer, it appears to us that the rejection of these claims is logically flawed on its face unless the examiner implicitly intends to further build upon the two previously stated rejections for claims 1-3 and 5-11. In the third and fourth stated rejection as to claims 12-17, the examiner's intent appears to merely add Sugiyama respectively to the first and second stated rejections.

Rather than repeat the positions of the appellant and the examiner, reference is made to the brief and the answer for the respective details thereof.

OPINION

We reverse.

As disclosed and depicted in specification Figure 6, in response to the generation of an insert signal from the insert key 8 in Figure 1, a pointing vector generator generates a block of pointing vectors 29 in Figure 6 having a respective first address signal (n) which specifies the location where dictated insert should be inserted in the data file (F), and a second address signal (p) which indicates the beginning address of an available portion of addressable memory for actually storing the insert itself. Although not set forth in independent claims 1 and 13 on appeal, a third address vector location (q) identifies the ending address of the dictated insert.

It is thus apparent that the dispute revolves around the stated first and second address signals generated by the claimed pointing vector generator means in representative independent claim 1 on appeal. Corresponding features are recited in independent claim 13 on appeal as well. It is this clause at the end of representative claim 1 on appeal that appellant rightly argues that the examiner has not proven to be taught or suggested among the prior art applied. Appellant's arguments do not dispute the proper combinability within 35 U.S.C. § 103 of the references relied upon, but only assuming a proper combination is

made, that all the features of the claimed invention, namely, the pointing vector generating means clause of representative independent claim 1 on appeal is not taught or suggested. We agree.

The examiner's reasoning relies entirely upon Bissonnette for this feature. His voice activated personal organizer is shown in Figure 2 to include an edit key which is unnumbered. Furthermore, we recognize that in accordance with the abstract, for the different functions attributed to this device, the user may have the ability to edit them by eliminating or correcting the data entered or entering new data. It appears that this latter feature of entering new data is considered by the examiner to be analogous to the claimed inserting feature.

According to the architecture of Bissonnette's device in Figure 1, the DRAM 22 stores the data. This memory is discussed briefly in the paragraph at the middle of column 6 and more extensively beginning at the bottom of column 7 through the end of column 8. We do not agree with the examiner's views as to the teachings at column 8 that Bissonnette teaches or otherwise suggests to the artisan within 35 U.S.C. § 103 the data

structures correlating to the block of pointing vectors which comprise the claimed first and second address signals. There is no teaching here, and none anywhere else in the drawings and text of Bissonnette, which correlates to the claimed first address signal corresponding to a address where a dictation insert should be placed in the data file comprising data compressed speech signals. There is also no second address signal as claimed corresponding to the beginning address of an available portion of the addressable memory in the DRAM 22 for storing the dictation insert itself. We reach this conclusion because there is no additional pertinent teaching or discussion of the editing functions generally noted with respect to Figures 4, 7, 8, 9 and 15-17 and the manner in which any editing or additional insert-type information is stored within the memory 22 itself.

The examiner has not convinced us that the data structures associated with memory 22 in Bissonnette correlate to the claimed pointing vectors comprising first address signals and second address signals as claimed. The examiner's additional comments at pages 2, 8 and 9 of the answer relating to general understandings in the memory art relating to pointers are noted.

To the extent the art well recognizes the use of pointers for storing and accessing memory in various data processing devices is generally well known, the features recited in independent claims 1 and 13 on appeal are much more specific than any generalization that can reasonably be made on the basis of the applied prior art. Neither the examiner's generalizations nor our review of Bissonnette indicates that pointers were generally used in the art to indicate a point in already dictated speech where an insert is to be placed and the location in memory where the insert is actually stored, both of which correlate to the claimed first and second address signals.

In view of the foregoing, the decision of the examiner rejecting independent claims 1 and 13 on appeal is reversed. According to the examiner's formulation of the various rejections, the additional prior art is relied upon for different features and not the disputed feature as appellant notes at page 6 of the brief. As such, the reversal is extended to the respective dependent claims, and the additional prior art fails

to make up for the disputed feature in independent claims 1 and 13 on appeal. Accordingly, the decision of the examiner rejecting all claims on appeal under 35 U.S.C. § 103 is reversed.

REVERSED

James D. Thomas Administrative Patent Judge	)	
Joseph L. Dixon Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
Howard B. Blankenship Administrative Patent Judge	)	

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