

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JON CHEEK, DERICK WRISTERS, and
MARK I. GARDNER

Appeal No. 2001-1545
Application No. 09/199,666

ON BRIEF

Before KRASS, DIXON, and BARRY, **Administrative Patent Judges**.
DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal under 35 USC § 134 from the examiner's final rejection of claims 1-7, 9, 10, and 26-34, which are all of the claims pending in this application.

We REVERSE.

Appellants' invention relates to a semiconductor structure having elevated silicide source/drain regions and metal gate electrode on nitride/oxide dielectric. An understanding of the invention can be derived from a reading of exemplary claim 34, which is reproduced below.

34. A semiconductor structure having a gate structure formed on a substrate, the gate structure comprising:

a first gate dielectric formed on the substrate;

a second gate dielectric formed on the first gate dielectric, separate from the first gate dielectric, and having a width about equal to the first gate dielectric;

a metal gate electrode formed on the second gate dielectric layer and having a width about equal to the first and second gate dielectrics; and

nitride spacers formed on the substrate and adjacent each of the first and second gate dielectrics and the metal gate electrode.

The prior art of record relied upon by the examiner in rejecting the appealed claims is as follows:

Chau et al. (Chau)	5,908,313	Jan. 01, 1999 (filed Dec. 31, 1996)
Shiozawa et al. (Shiozawa)	5,970,352	Oct. 19, 1999 (filed Apr. 23, 1998)
Thomas et al. (Thomas)	6,004,878	Dec. 21, 1999 (filed Feb. 12, 1998)

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Claims 1-7, 9, 10, and 26-34 stand rejected under 35 U.S.C. § 103 as being unpatentable over Chau in view of Thomas and Shiozawa.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 14, mailed Jan. 19, 2001) for the examiner's reasoning in support of the rejections, and to appellants' brief (Paper No. 13, filed Dec. 1, 2000) for appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by appellants and the examiner. As a consequence of our review, we make the determinations which follow.

35 USC § 103

To reject claims in an application under section 103, an examiner must show an unrebutted *prima facie* case of obviousness. **See In re Deuel**, 51 F.3d 1552, 1557, 34 USPQ2d 1210, 1214 (Fed. Cir. 1995). In the absence of a proper *prima facie* case of obviousness, an applicant who complies with the other statutory requirements is entitled to a patent. **See In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.

In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1455 (Fed. Cir. 1998). Here, appellants argued that neither Chau nor Thomas evidences the claimed second gate dielectric formed on the first gate dielectric beneath a metal gate electrode in a semiconductor structure. (See brief at page 3.) The examiner maintains that Chau teaches at col. 5, lines 26-29, that the language of “other well known gate dielectrics such as oxides, nitrides and combinations thereof may be utilized” for the gate electrode. The examiner maintains that other well known combinations of oxides and nitrides include multi-layer dielectrics not specifically shown in Figure 3E and that this teaching of Chau alone would have suggested the claimed layers. (See answer at pages 3-4.) In the alternative, the examiner relies upon the teachings of Thomas with respect to Figure 6 and description at col. 3 of the gate dielectric layer 40. The examiner acknowledges that neither Chau nor Thomas expressly show the gate dielectric layer as having two layers, but relies upon the language in the descriptions to suggest that there would be two layers in alternative embodiments. (See answer at pages 3-4.)

Appellants argue that the examiner has not shown in the prior art applied, the use of multiple separate layers for the gate dielectric. (See brief at page 4.) We agree with appellants, and we do not find that the examiner has shown or provided a

convincing line of reasoning why it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the single layer of gate dielectric as multiple layers of dielectric. The examiner provides various rationales of using plural dielectric layers at pages 4-5 of the answer, but provides no teaching or suggestion in the prior art applied. Additionally, the examiner maintains that the combination of layers comprising silicon oxide and silicon nitride, “is an art recognized equivalent to a conventional gate dielectric layer such as single layers of silicon oxide, silicon nitride, silicon oxynitride etc.” (See answer at page 5.) The examiner and Board may not, because of doubt that the invention is patentable, resort to speculation, unfounded assumption or hindsight reconstruction to supply deficiencies in the factual basis for the rejection. **See In re Warner**, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), **cert. denied**, 389 U.S. 1057 (1968). Here, the examiner has provided no evidence of the asserted equivalence, and we will not speculate whether the equivalence is well founded in the relevant prior art. The examiner maintains that the language of Chau suggests multiple layers to be used in place of the oxynitride gate dielectric layer and argues that grammar dictated the language used in the recitations in Chau. (See answer at page 7.) We are not persuaded by the examiner’s arguments and find that

Chau references a single “layer” throughout the disclosure, and we find no clear and convincing rationale to use two layers to replace the single layer disclosed by Chau.

Similar argument is made alternatively by the examiner concerning the teachings of Thomas. (See answer at page 8.) Here, the examiner maintains that Thomas teaches and suggests the use of plural layers of dielectric based upon the language that the “gate dielectric layer 40 can be formed as a composite layer of silicon oxide and silicon nitride.” (See answer at page 8 and Thomas at Col. 3.) The examiner relies on the term “composite” as being defined as “made up of distinct parts.” While we agree that a composite may be separate layers, we do not find that Thomas teaches or suggests the use of plural distinct layers since Thomas merely references a single “layer” in the disclosure. The examiner maintains that the motivation for using two dielectric layers can come from knowledge generally in the art. (See answer at page 9.) While we agree with the examiner that the motivation can come from knowledge in the art, we find that the examiner has not established what the level of skill in the relevant art would have been nor has the examiner provided any teaching of the asserted equivalence of the one layer dielectric and the two layer dielectric.

Since the examiner has not provided a teaching or convincing line of reasoning supported by evidence suggesting that the single layer dielectric of Chau or Thomas be replaced by two layers of dielectric, and since the examiner does not rely on the

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teachings of Shiozawa to teach or suggest the use of two dielectric layers, we will not sustain the rejection of independent claim 34. Since independent claims 1 and 33 contain similar limitations directed to the use of two gate dielectric layers, we will similarly not sustain the rejections of these claims and their dependent claims 2-7, 9, 10 and 26-31.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1-7, 9, 10, and 26-34 under 35 U.S.C. § 103 is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH L. DIXON)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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LANCE LEONARD BARRY)	
Administrative Patent Judge)	

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