The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 12

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MAUREEN A. HANRATTY,
DATY M. ROGERS, QIZHI HE,
and WEI WILLIAM LEE

Appeal No. 2001-1814
Application 09/092,115

ON BRIEF

Before KRASS, JERRY SMITH, and BARRY, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-4, which constitute all the claims in the application.

The disclosed invention pertains to a method of integrated circuit fabrication with transistor gates having a gate length less than the linewidth provided by the lithography

in conjunction with interconnects or gate tops with linewidth as provided by the lithography. This method allows the typically smallest linewidth (the gate length) to be sublithographic in conjunction with standard lithography.

Representative claim 1 is reproduced as follows:

1. A method of fabrication of an integrated circuit, comprising the steps of:

(a) patterning a first layer of resist on a layer of gate material to define gate locations;

(b) reducing the linewidth of said patterned layer of resist of step (a);

(c) using said reduced linewidth patterned resist as an etch mask to form gates from said layer of gate material;

(d) forming a layer of dielectric on said gates;

(e) patterning a second layer of photoresist to define interconnects;

(f) using said patterned photoresist without linewidth reduction to form interconnects over said gates.

The examiner relies on the following references:

Auda et al. (Auda)	5,139,904	Aug. 18, 1992
Maniar et al. (Maniar)	5,525,542	June 11, 1996
Mishra et al. (Mishra)	5,798,555	Aug. 25, 1998 (filed Nov. 27, 1996)

S. Wolf, “Silicon Processing for the VLSI Era Volume 2 - Process Integration,” 1986, pages 278-286.

Claims 1-4 stand rejected under 35 U.S.C. § 103. As evidence of obviousness the examiner offers the combination of Auda and Wolf with respect to claims 1-3 and the combination of Mishra, Auda and Maniar with respect to claim 4. The double patenting rejection of claim 1 which was made in the final rejection has been withdrawn by the examiner [answer, page 7].

Rather than repeat the arguments of appellants or the examiner, we make reference to the brief and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the brief along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in

the art the obviousness of the invention as set forth in claims 1-4. Accordingly, we affirm.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness.

Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See Id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the brief have not been considered and are deemed to be waived [see 37 CFR § 1.192(a)].

We consider first the rejection of claims 1-3 based on the teachings of Auda and Wolf. These claims stand or fall together as a single group [brief, page 3]. The examiner cites Auda as teaching a method of fabrication of an integrated circuit which meets the claimed invention except that Auda does not explicitly disclose a patterned photoresist without linewidth reduction to form interconnects over the gates. The examiner notes, however, that these conventional processes are notoriously obvious as shown by Wolf. The examiner asserts that because

there is no need to reduce the linewidth of interconnect areas of the circuit, the artisan would have employed standard etching techniques which would yield unreduced linewidth patterns. Thus, the examiner finds that it would have been obvious to the artisan to use reduced linewidth patterns on the gates as taught by Auda but to use conventional linewidth lithography on the interconnects as taught by Wolf [answer, pages 3-5].

Appellants argue that Auda would inherently use the same photoresist linewidth reduction to the interconnect formation as to the gate formation. In other words, appellants argue that the applied prior art fails to teach the use of both reduced and nonreduced linewidths [brief, page 3].

The examiner responds that Wolf shows that linewidths of the gate electrode and the CVD tungsten interconnect are different. The examiner asserts that the use of a reduced linewidth would not be necessary in the formation of the CVD tungsten interconnect as compared to the gate electrode in Wolf's Figure 4-58. The examiner notes that the applied prior art only teaches a reduced linewidth for the gate electrodes [answer, page 7].

We will sustain the examiner's rejection of claims 1-3. Appellants' argument that Auda would inherently apply the same

photoresist linewidth reduction to the interconnect formation as to the gate is not convincing. Auda teaches the use of linewidth reduction in the formation of FET gates because it permits the miniaturization of such FET devices. We agree with the examiner, however, that similar linewidth reduction is not necessary in forming interconnect lines between components. There is no reason why the artisan would go to the extra effort of reducing linewidths where such reduction serves no specific purpose. The collective teachings of the applied prior art teach that the linewidths resulting from conventional lithography should be reduced in the formation of gates. There is no similar teaching that the formation of interconnects should have similarly reduced linewidths. Appellants' argument that there is no suggestion of using reduced and nonreduced linewidths in the same device is, therefore, not persuasive.

We now consider the rejection of claim 4 based on the teachings of Mishra, Auda and Maniar. The examiner's rejection is explained on pages 5-6 of the answer. Appellants again argue that the references have no suggestion of the mixed use of photoresist with and without linewidth reduction. Appellants argue that Mishra is inconsistent with Auda and the references fail to suggest the claimed combination [brief, pages 3-4]. The

examiner responds that Auda suggests the use of reduced photoresist in forming short channel polysilicon gate FETs but does not suggest this technique in the formation of the conventional interconnects. The examiner notes that it would be implausible to use reduced photoresist for conventional interconnects without any explicit motivation [answer, pages 7-8].

We will sustain the examiner's rejection of claim 4. We are not persuaded by appellants' argument that the applied references are inconsistent. The examiner is using Auda as motivation to reduce the gate linewidth of Mishra for the advantages disclosed by Auda. We agree with the examiner's argument that Auda only teaches linewidth reduction with respect to the gate and does not suggest such reduction for the interconnects as well.

In summary, we have sustained the examiner's rejection of each of the claims on appeal. Therefore, the decision of the examiner rejecting claims 1-4 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

ERROL A. KRASS Administrative Patent Judge	)	
JERRY SMITH Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

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