

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte RAVISHANKAR KUPPUSWAMY  
and GREGORY TAYLOR

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Appeal No. 2001-1955  
Application 08/989,917

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ON BRIEF

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Before THOMAS, FLEMING, and DIXON, Administrative Patent Judges.  
THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1-10 and 19-30. Claims 11-18 have been canceled. Because the examiner has indicated at page 2 of the answer that rejections from this final rejection under the both first and second paragraphs of 35 U.S.C. § 112 have been withdrawn, claims 1-10 and 19-29 remain on appeal. The examiner's statement at page 2 of the answer that claims 1-10 and 19-28 remain on appeal is incorrect.

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Representative claim 1 is reproduced below:

1. A delay element, comprising:

an input that receives an input signal,

an output,

a plurality of delay stages mutually interconnected in a cascaded relationship, each stage imposing an incremental delay upon the input signal when included in a path of propagation of the input signal between the input and the output, and

a second input that receives a selection signal, the selection signal determining how many of the delay stages are included in the path of propagation.

The following reference is relied on by the examiner:

McKinney

5,389,843

Feb. 14, 1995

Appellants note at the bottom of page 2 of the principal brief on appeal that a second amendment after final was filed with the brief. As noted at page 1 of the reply brief, the examiner has not indicated in the answer the entry of this amendment. For purposes of rendering a decision on this appeal, we consider this amendment to have been entered since it appears to us not to affect the nature of the remaining rejections of the claimed on appeal.

As noted earlier, there is no rejection before us of claim 30 on appeal. Appellants correctly note at the top of page 2 of the principal brief on appeal that claims 1 and 19-23 stand

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rejected under 35 U.S.C. § 102(b) as being anticipated by McKinney. Claims 2-10 and 24-29 are also noted at the top of page 2 of the reply brief to be rejected under 35 U.S.C. § 103.

Rather than repeat the positions of the appellants and the examiner, reference is made to the briefs and the answer for the respective details thereof.

#### OPINION

For the reasons set forth by the examiner in the answer as amplified upon here, we sustain the rejection of claims 1 and 19-23 under 35 U.S.C. § 102. Of the remaining claims on appeal, claims 2-10 and 24-29, we sustain only the rejection of claims 2, 6-10 and 24-29.

Turning first to the rejection of claims 1 and 19-23 under 35 U.S.C. § 102 as being anticipated by McKinney, appellants' arguments with respect to independent claim 1 at pages 8 and 9 of the principal brief on appeal as well as those set forth as to this claim at page 2 of the reply brief focus upon the view best expressed at the top of page 2 of the reply brief that "because the input SIGNAL traverses at least a portion of every stage in McKinney's circuit, McKinney does not teach or disclose a

'selection signal determining how many of the delay stages are included in the path of propagation' as is required by claim 1." Although this view has some merit when considering the labeled stages 1-N of McKinney's figure, we are persuaded to affirm this rejection by the examiner's views expressed at page 6 of the answer that the claimed delay stages are met by the reference when each of the respective stages 1-N is considered in the context of the delay elements 10-20-80 as comprising the claimed delay stages. By the use of the delay select bits LSB-MSB feeding the respective multiplexers 12, 22 and 82 in McKinney's figure, a selection signal is provided that determines how many of the respective delay stages, that is, the delay elements 10-20-80, are included in the path of propagation for the SIGNAL, its input on the left to its output on the right. From our perspective, what is telling is not whether the examiner may interpret a given claim with respect to the teachings and showings in McKinney different as to one claim verses another claim, but what the reference actually teaches in total with respect to any given independent claim, for example, on appeal.

We are equally unpersuaded by appellants' arguments at pages 7 and 8 of the principal brief on appeal regarding independent claim 23. Appellants' assert at the top of page 8 and again at

page 2 of the reply brief that McKinney does not show a single delay stage as a first delay stage of the claim being "connected" to both the input terminal and the output terminal of a delay tuning circuit.

At the outset, it is apparent to us that appellants considered claim 23 to recite only a single delay stage that is respectively connected to the input and output terminal claimed by the manner in which the claim is argued. They therefore apparently concede that the claimed plurality of mutually interconnected delay stages are met to the extent also recited in claim 23 on appeal. The claim does not recite whether the plurality of stages are connected in series or in parallel or any manner in which they are interconnected. What appellants appear to be arguing with respect to claim 23 and its single delay stage that is argued is that there appears to no "direct connection." Since this is not claimed, the claim is clearly met by a simple inspection of the figure of McKinney. Each of the respective labelled stages 1-N in McKinney's figure are clearly "connected" to each other from an input on the left to an output on the right. Additionally, the teachings of the plurality of stages "stages 1-N" as labeled in McKinney encompass the teaching that one or only one stage may be present in the overall circuit

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depending upon use. Even if there are only two or a plurality of interconnected stages, at least one stage is connected in the manner claimed to the extent it is recited in the claim.

Independent claims 19 and 21 are respective method and method of manufacturing claims reciting essentially the same subject matter between them. McKinney does disclose in our view a data circuit in his drawing figure that includes a plurality of cascaded delay stages 1-N which may be selected for inclusion in a path of propagation of the output signal based on the value of a selection signal. We agree with the examiner's view that claims 19 and 21 are met by the teachings and showings in McKinney since this reference essentially does vary the nature of the selection signal until the path of propagation imposes a desired delay upon the output signal which is essentially therefore fixed because the reference's aim as expressed in the initial paragraph at column 1 of McKinney's patent is to provide a programmable variable length delay circuit. It is clearly going to be programmed or varied to the extent the desired delay is achieved, and therefore it is programmed or fixed once that delay is achieved.

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As expressed at page 9 of the principal brief on appeal, the rejection of claim 22 relies on similar arguments as with respect to claims 19 and 21. Therefore, we have sustained the rejection of claim 22 as well.

Turning lastly to the rejection of claims 2-10 and 24-29 under 35 U.S.C. § 103 as being obvious over McKinney alone, we sustain only the rejection of claims 2 and 6-10 as well as 24-29.

We reverse the rejection of claims 3 and 4 since we are persuaded by the substantive arguments presented by appellants at page 10 of the principal brief on appeal as to these claims. The mere functional equivalence argued by the examiner at page 8 of the answer relating to the delay buffer 10, 20 and 80 of McKinney's figure does not fully address the requirement of claims 3 and 4 as noted at the top of page 10 of the principal brief on appeal that a delay block having two inputs is required. McKinney's delay buffers 10-20 and 80 do not have such a dual input. Similarly, McKinney does not teach or show the use of inverted buffers as recited in claim 3. Because claim 5 depends from claim 3, we must reverse the rejection of claims 3-5.

No arguments are presented for our consideration as to claims 2, 6-8 and 10. As to claim 9, appellants' mere recognition or repetition of what the examiner has said is not

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taught in his rejection under 35 U.S.C. § 103 as to claim 9 as expressed at the bottom of page 9 of the principal brief on appeal is misplaced. The mere fact that the examiner has asserted that McKinney does not disclose a decoder as in claim 9 is an incomplete statement of the examiner's view expressed at page 5 of the answer. Although we are not persuaded by the examiner's assertion that the use of decoders was well known in the art and such therefore renders claim 9 obvious within 35 U.S.C. § 103, the reference still teaches or suggests to the artisan this claimed circuit element anyway. The discussion of the prior art patent to Ramsey at column 1 of McKinney specifically mentions that decoders are contemplated within the context of his teachings as noted in the sentence at lines 33-37. The summary of the invention of McKinney that follows this discussion clearly indicates to us and to the artisan that McKinney's 2-input multiplexers 12-22-82 in his figure perform in essence a decoding operation or function.

As noted by the examiner at the bottom of page 7 of the answer, appellants predicate patentability of claims 24-28 on the basis of their urging the patentability of claims 1 and 23. Therefore, no separate arguments are presented to these claims in the principal brief on appeal. To the extent appellants make

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mention of claim 24 at the top of page 3 of reply brief, arguments as to this claim in the reply brief will not be entertained by us since no arguments have been presented in the principal brief on appeal. Since the examiner is not permitted to respond to the reply brief under the current rules of practice, the arguments directed to claim 24 in the reply brief are inappropriate and will not be considered.

Lastly, we address independent claim 29 on appeal. Appellants recognize at the top of pages 2 and 5 of the principal brief on appeal that claim 29 is rejected under 35 U.S.C. § 103. This is clear from the top of page 6 of the final rejection, the middle of page 5 of the answer and the top of page 9 of the answer. However, there are no arguments presented in the brief or reply brief as to claim 29. As such, appellants appear to concede the unpatentability of this claim under 35 U.S.C. § 103. We note in passing that this claim appears to read on appellants' recognized prior art approach as into prior art Figure 3.

In summary, we have sustained the rejection of independent claims 1, 19, 21, 22 and 23 under 35 U.S.C. § 102. Because appellants have also presented no arguments as to dependent claim 20, this claim falls with its parent independent claim 19. Of

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claims 2-10 and 24-29 rejected under 35 U.S.C. § 103, we have sustained only the rejection of claims 2, 6-10, and 24-29. Therefore, the decision of the examiner rejecting various claims on appeal under 35 U.S.C. § 102 and 35 U.S.C. § 103 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

James D. Thomas	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
Michael R. Fleming	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
	)	INTERFERENCES
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Joseph L. Dixon	)	
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