

The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEVEN WAYNE WHITE, HUNG QUI LE and
KURT ALAN FEISTE

Appeal No. 2001-2610
Application No. 09/052,247

ON BRIEF

Before KRASS, BLANKENSHIP and SAADAT, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1, 8-13, 27 and 33.

The invention pertains to instruction prefetch in a data processing system.

Appeal No. 2001-2610
Application No. 09/052,247

Fetching units first look to the cache for the next needed instruction in a set of instructions. If the instruction is not in the cache, this is termed a "cache miss" and the fetching unit must then retrieve the instruction from the system memory. As processor clock rates increase more rapidly than memory access times do, the latency penalties from a cache miss increase accordingly.

Memory latency due to a cache miss may be reduced by prefetching an instruction cache line from a system memory device. The problem is that if an instruction that alters an instruction sequence path is executed, the prefetched cache line may not be used because an instruction may cause a jump to an instruction path that is outside the prefetched cache line. Prefetching a cache line that is not used leads to "cache pollution" and this reduces the effectiveness of prefetching.

The present invention is directed to a prefetch mechanism that permits cache miss requests to be issued earlier without increasing cache pollution.

Representative independent claim 1 is reproduced as follows:

1. In a data processor, a method of reducing cache miss penalties comprising the steps of:

Appeal No. 2001-2610
Application No. 09/052,247

determining if a fetched instruction is an instruction-path-changing instruction; and

if said fetched instruction is not an instruction-path-changing instruction, prefetching a next sequential preselected instruction set if no remaining instructions in a current cache line are not path-changing instructions, wherein an instruction-path-changing instruction branches beyond said next sequential preselected instruction set.

The examiner relies on the following reference:

Mahalingaiah et al. [Mahalingaiah] 5,813,045 Sep. 22, 1998
(filed Jul. 24, 1996)

Claims 1, 8-13, 27 and 33 stand rejected under 35 U.S.C. 102(e) as anticipated by Mahalingaiah.

Claims 2-7, 14-26 and 28-32 have been indicated by the examiner to be directed to allowable subject matter and are no longer on appeal.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

An anticipatory reference is one which describes all of the elements of the claimed invention so as to have placed a person of ordinary skill in the art in possession thereof. In re Spada, 911 F.2d 205, 15 USPQ2d 1655 (Fed. Cir. 1990).

Appeal No. 2001-2610
Application No. 09/052,247

Taking claim 1, as exemplary, the examiner points to column 8, lines 47-49, of Mahalingaiah as a teaching of determining if a fetched instruction is an instruction-path-changing instruction because the prefetch/predecode unit determines the branch target of a line being predecoded. The examiner points to column 8, lines 65-67, of the reference for a teaching of if the instruction is not path-changing, then prefetching a next sequential instruction, because the cited portion discloses a branch direction being "taken," in which subsequent instructions are fetched from the target address of the branch instruction, wherein the target address of a branch instruction is known to be beyond the next sequential address.

Appellants contend that there is nothing in Mahalingaiah that teaches determining if a fetched instruction is an instruction-path-changing instruction in which an instruction-path-changing instruction branches beyond the next sequential instruction set. Further, contend appellants, the examiner has identified no teaching in the reference disclosing that the target branch of a branch instruction is known to be beyond the next sequential address and there is no reason for the target address of a branch instruction to necessarily be beyond the next sequential address in a cache line [principal brief-page 6].

Appeal No. 2001-2610
Application No. 09/052,247

With regard to independent claim 27, the examiner asserts that Mahalingaiah teaches, at column 7, lines 63-65, that the start and end predecode bits indicate the boundaries of the prefetched instruction, therefore designating the range of desired data values to be accessed, meeting the language of claim 27 which requires that prefetching is done in response to the predecode bits, and not in response to the predecode bits having a preselected value [answer-page 9].

It is appellants' position that Mahalingaiah does not disclose predecode bits, which, in response thereto, a next sequential instruction set is prefetched into an instruction storage device.

We have carefully reviewed the evidence before us, including, inter alia, the arguments of appellants and the examiner, and we conclude that, to whatever extent the examiner has set forth a prima facie case of anticipation, appellants have made arguments that raise serious doubts about Mahalingaiah anticipating the instant claimed subject matter. Accordingly, we will not sustain the rejection of claims 1 and 27, or of claims 8-13 and 33, dependent therefrom, under 35 U.S.C. 102(e).

Turning, first, to independent claim 1, we note, initially, that we find the double negative language, "if no remaining

Appeal No. 2001-2610
Application No. 09/052,247

instructions in a current cache line are not path-changing instructions," to be a little confusing. Apparently, however, appellants and the examiner have no trouble with this language.

The main language in issue with regard to claim 1 is "wherein an instruction-path-changing instruction branches beyond said next sequential preselected instruction set." We agree with appellants that Mahalingaiah does not appear to teach the determination if a fetched instruction is an instruction-path-changing instruction in which the instruction-path-changing instruction branches beyond the next sequential address. The examiner relies on column 8, lines 65-67, of Mahalingaiah, wherein the reference recites that the branch direction may "not be taken", in which subsequent instructions are fetched from memory locations consecutive to the branch instruction. We fail to see how this is a teaching of "wherein an instruction-path-changing instruction branches beyond said next sequential preselected instruction set." As explained by appellants, at pages 3-4 of the reply brief, "a teaching directed to the branch being taken, if the branch target is beyond the next sequential instruction, is an instruction-path changing instruction. Therefore, teaching in *Mahalingaiah* directed to the branch being taken, is inapplicable to a limitation directed to the step of

Appeal No. 2001-2610
Application No. 09/052,247

prefetching a next sequential instruction if the instruction *is not an instruction-path changing instruction.*"

Moreover, it is our view that the examiner's rationale for the rejection of claim 1 is flawed because the examiner states [answer-page 4] that "if the instruction is not path-changing, then prefetching a next sequential instruction by [Mahalingaiah's] teaching in column 8, lines 65-67 of the branch direction being "taken", in which subsequent...instructions are fetched from the target address of the branch instruction, wherein the target address of a branch instruction *is known* to be beyond the next sequential address" [emphasis ours]. We find no rational basis for the statement that the target address of a branch instruction "is known" to be beyond the next sequential address. We agree with appellants that it is possible that a target address of a branch instruction may be beyond the next sequential address but the mere fact that a certain thing *may* result from a given set of circumstances is not sufficient to show that the reference describes the limitation in claim 1 directed to instruction-path-changing instructions [reply brief-pages 4-5]. The claim does not merely state that a target address branches beyond a next sequential address. It requires that an "instruction-path-changing instruction," (i.e., an

Appeal No. 2001-2610
Application No. 09/052,247

instruction which may, itself, direct a branch to be taken if the branch target is beyond the next sequential instruction), branches beyond said "next sequential preselected instruction set" so it is unclear how the branch taken in Mahalingaiah is directed to the prefetching of a next sequential instruction if the instruction is not an instruction-path-changing instruction.

With regard to claim 27, this claim specifically recites the prefetching of "a next sequential instruction set...in response to said predecode bits." The examiner relies on column 7, lines 63-65, of Mahalingaiah for this teaching. That portion of the reference recites that the "predecode bits form tags indicative of the boundaries of each instruction." While this may designate the range of desired data values to be accessed, as alleged by the examiner [answer-page 9], it indicates nothing about prefetching a next sequential set "in response to" predecode bits, as required by the instant claim language. Accordingly, since the examiner has not shown how, or where, every claim limitation is shown in the reference, we will not sustain the rejection of claim 27 under 35 U.S.C. 102(e).

Appeal No. 2001-2610
Application No. 09/052,247

The examiner's decision rejecting claims 1, 8-13, 27 and 33
under 35 U.S.C. 102(e) is reversed.

REVERSED

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| ERROL A. KRASS |) | |
| Administrative Patent Judge |) | |
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| HOWARD B. BLANKENSHIP |) | BOARD OF PATENT |
| Administrative Patent Judge |) | APPEALS AND |
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| |) | |
| MAHSHID D. SAADAT |) | |
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Appeal No. 2001-2610
Application No. 09/052,247

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