The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GEORGE MCNEIL LATTIMORE, DONALD GEORGE MIKAN JR., JOSE ANGEL PAREDES and GUS WAI-YAN YEUNG

Appeal No. 2002-0140
Application No. 09/435,864

ON BRIEF

Before KRASS, RUGGIERO and DIXON, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-4, 6, 7, 9, 14, 15 and 17. Claims 5, 8, 10-13, 16 and 18 stand allowed by the examiner.

The invention is directed to multi-staged circuits which use multi-clocks for timing between stages. These circuits have an undeterminable clock underlap problem brought about by

insufficient triggering of the rising and falling edges of an output signal. The instant invention, rather than relying on a first clock for triggering both the rising and falling edge of the output, utilizes a second clock in the first stage for triggering the falling edge of the output. This second clock also controls the second stage output.

Representative independent claim 1 is reproduced as follows:

1. A method for dealing with an unspecific underlap requirement in timing-sensitive dynamic circuits of a multi-clocked system comprising:

receiving a first clock signal in a first stage;

controlling an output from the first stage using the first clock signal; and

receiving a second clock signal in the first stage;

controlling the output from the first stage using the second clock signal.

The examiner relies on the following references:

Wu et al. (Wu)	5,378,942	Jan. 3, 1995
Levy et al. (Levy)	5,825,208	Oct. 20, 1998

In addition, the examiner relies on admitted prior art (APA) depicted in instant Figures 1 and 3.

Claims 1-4 and 6 stand rejected under 35 U.S.C. § 102(b) as

anticipated by Wu. Claims 9, 14, 15 and 17 stand rejected under 35 U.S.C. § 102(b) as anticipated by Levy. Claim 7 stands rejected under 35 U.S.C. § 103 as unpatentable over Wu in view of APA.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

Under 35 U.S.C. § 102(b), a reference must disclose, explicitly or implicitly, every limitation of the claimed invention. Glaxo Inc. v. Novopharm Ltd., 52 F.3d 1043, 1047, 34 USPQ2d 1565, 1567 (Fed. Cir.), cert. denied, 516 U.S. 988 (1995).

With regard to claims 1 and 2, the examiner applies Wu as follows: In Figure 1 of the reference, the first stage is considered to be logic gates 10 and 11, with the first clock signal at phase 34. The second clock signal is considered to be phase 3. Since both of these clock signals are received in the first stage, the claim limitations of "receiving a first clock signal in a first stage" and "receiving a second clock signal in the first stage" are met. Moreover, since the output of the first stage, e.g., at point V3, is determined by application of

the clock signals phase 3 and phase 34, it is clear that the output of the first stage is controlled using the first and second clock signals, as claimed.

With regard to instant claim 2, it is also clear that the second clock signal, phase 3, is also received in a second stage, logic gates 12 and 13, and the output of the second stage, Vout, is controlled using this second clock signal.

It appears to us that the examiner has indeed established a prima facie case of anticipation with regard to the subject matter of instant claims 1 and 2.

For their part, appellants contend that Wu does not teach the features of controlling the outputs of the first and second stages using the second clock signal. For the reasons supra, we disagree. If the clock signal has an effect on the output, it may be said to "control" the output.

Appellants also contend that the output of Wu's circuit is not controlled by an output from a first stage using a first clock signal, but instead, is controlled by the skew effect of the transistors. Appellants further explain that the circuits of Wu "use the same clocks...but change both the way the transistors are connected throughout the circuit as well as reducing the

number of transistors in the circuit" (brief-page 5). We are unsure of the point appellants are making. If the clock signals control the transistors and the skew effect of the transistors control the output, it seems clear that the clock signals control the output.

In any event, we suspect appellants are not considering the breadth of the claims at issue. For example, all that is required by claim 1 is that both a first and second clock signal be received by the first stage (clearly, stage 11 in Wu receives both a clock signal phase 34 and a clock signal phase 3) and that an output of the first stage is controlled using both the first and second clock signals (since both clock signals are input in the first stage in Wu and the output is dependent on those clock signals, it is clear that the first stage is controlled by the clock signals). Accordingly, Wu is seen to anticipate the subject matter claim 1, as well as claim 2.

It is noted that nowhere do appellants argue or deny that Wu is directed to a method for dealing with an unspecified underlap requirement in timing-sensitive dynamic circuits of a multi-clocked system, as claimed. The problem of "clock-skew race," described by Wu, appears to be the same problem to which the instant claimed subject matter is directed.

Accordingly, we will sustain the rejection of claims 1 and 2 under 35 U.S.C. § 102(b).

We turn, now to the rejection of claims 3, 4 and 6.

Claim 3 requires "triggering a rising edge of the output using a rising edge of the first clock signal" and claim 4 requires "triggering a falling edge of the output using a rising edge of the second clock signal."

The examiner's answer refers to Figure 7 of Wu for these limitations and, Figure 7 being an electrical schematic diagram of a logic structure with no waveforms shown, appellants understandably argue that it is "not clear" how the reference to Figure 7 in Wu indicates using a rising edge of the second clock signal to trigger a falling edge of the output or stabilizing the output.

We, too, have a bit of trouble discerning how Figure 7 of Wu indicates the claimed limitations. However, reference to Figure 3, a timing diagram for the circuitry of Figure 1, makes it a bit clearer.

If we focus on clock signals phase 3 (second clock signal) and 34 (first clock signal) and output V3, the diagram in Figure 3 clearly shows a rising edge of the output V3 (near the arrow

head of line 16) being triggered in response to a rising edge of the first clock signal phase 34, as required by instant claim 3. Moreover, the figure also shows a falling edge of output V3 being triggered by a rising edge of second clock signal phase 3. With regard to stabilizing the output, as recited in claim 6, that appears to be the purpose of Wu in solving the clock-skew race problem.

Accordingly, we will sustain the rejection of claims 3, 4 and 6 under 35 U.S.C. § 102(b).

We now turn to the rejection of claims 9, 14, 15 and 17 under 35 U.S.C. § 102(b) as anticipated by Levy.

The examiner applies Figure 5 of Levy to independent claim 9 as follows:

The claimed first stage comprises a logic device 516 with at least one output, at line 517. A first transistor Q3 is connected to a first clock source 530 at a first transistor gate wherein the first transistor drain is connected to an output port of the logic device. A second transistor 512 is connected to a second clock source 528 at a second transistor gate, wherein the second transistor drain is connected to the first transistor at a first transistor source. A second stage 522 is connected to the first stage for receiving the first stage output from inverter

518.

Appellants' only argument in this regard is that the first transistor is **not** connected to an output port of the logic device 516 in Levy, as required by the language of claim 9.

While we understand the difference between the instant invention and that disclosed by Levy, the instant claim language does not require a **direct** connection. The connection of transistor Q3 in Levy to output port 517 **through** logic device 516 is not precluded by the instant claim language.

Accordingly, we will sustain the rejection of claim 9, and of claims 14, 15 and 17, dependent thereon, since appellants do not separately argue the merits of these claims, under 35 U.S.C. § 102(b).

Finally, we turn to the rejection of claim 7 under 35 U.S.C. § 103.

Claim 7 depends from claim 1 through claim 6 and adds the further limitation that stabilizing the output further comprises "creating a full keeper, wherein the full keeper holds the output."

The examiner's position is that while Wu does not disclose such a "full keeper," APA shows such a full keeper at I106, P108 and N106, connected to an output of a stage for the purpose of

latching the output and that it would have been obvious "to have coupled a full keeper to the output of the first stage of Wu as

taught by applicant's prior art figure 3 for the purpose of latching the output signal" (answer-page 5)

Appellants argue that there is no indication, in Wu, of a desirability of coupling the output of a first stage in Wu and a full-keeper. Further, appellants argue, making such a combination would destroy the intended logic circuit operational speed enhancement method of Wu by the addition of extra circuit components since these extra components would "degrade its operational speed" (brief-page 10). Appellants contend that Wu "teaches away" from the proposed combination because it would degrade the performance of the circuit described in Wu by slowing the operational speed of the circuit as a whole.

We agree with the examiner that it would have been obvious to provide for a full-keeper in Wu for the same reasons a full-keeper is employed in prior art systems, such as shown in APA. The advantage of a full-keeper for stabilization and connected to an output of a logic gate for the purpose of latching the output signal was well known, as depicted in APA and appellants do not contend otherwise. Therefore, the artisan would have been well

aware of the advantages and sought to include such a full-keeper in other logic structure, e.g., as in Wu.

While it may be that the addition of this circuitry in Wu might slow down performance, this is not, necessarily, a "teaching away" because the artisan might well accept a bit slower performance for the added benefits of a full-keeper for latching an output signal.

Accordingly, we will sustain the rejection of claim 7 under 35 U.S.C. § 103 in view of the prima facie case of obviousness made out by the examiner and the lack of convincing rebuttal by appellants.

The decision of the examiner rejecting claims 1-4, 6, 9, 14, 15 and 17 under 35 U.S.C. § 102(b) and claim 7 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

ERROL A. KRASS Administrative Patent Judge	)	
JOSEPH F. RUGGIERO Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JOSEPH L. DIXON Administrative Patent Judge	)	

EK/RWK

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