Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte HANS-JURGEN REUMERMAN, THOMAS MEUSER,
VEIT PIETZUCH and KAI KLAPDOHR

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Appeal No. 2002-1044
Application No. 09/017,096

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ON BRIEF

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Before BARRETT, FLEMING and BLANKENSHIP, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 10-13, 15, 20-22, 24 and 25. Claims 1-9 has been canceled. Claims 14, 16-19, 23 and 26-30 are objected to as being dependent upon a rejected base claim that would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.[1]

[1] See Examiner's answer, page 6.

Invention

The invention relates to a coupling device (switch) for a local network operating in the asynchronous transfer mode (ATM) which comprises a central cell memory for buffering packets formed by individual ATM cells. See page 1 of Appellants' specification. The entire coupling device (switch) is shown in Figure 4. A central memory control device 40 receives ATM cells over the feed lines 43 and provides them to the monitoring device 41 which evaluates the cell's header, and to the gate 42. The gate 42 receives discard signals from the gate 8 of the control logic 44 and sends the cells, which are not to be discarded to the central cell memory 45. See Appellants' specification, page 9.

Independent claim 10 is representative of the Appellants' claimed invention and is reproduced as follows:

> 10. A coupling device, for a network operating in the asynchronous transfer mode (ATM), comprising:
>
> means for receiving individual ATM cells each having a respective header,
>
> a central cell memory for buffer storage of packets formed by said individual ATM cells,
>
> a central memory control device for controlling storage in the central cell memory and the writing and reading processes for packets stored in and read from the central cell memory,

counting means for a number of ATM cells stored in said central cell memory, and

discarding means for discarding ATM cells packet by packet to prevent congestion in the central cell memory,

characterized in that the central memory control device comprises:

comparator means connected upstream of the central cell memory, and

control logic means,

said comparator means cooperating with the counting means and the control logic means such that, responsive to a programmable threshold value for the degree of filling of the central cell memory being reached, and evaluation of information determinable from the header of a received cell relating to the packet of which the received cell is a part, each ATM cell of the packet containing said received cell is discarded before arriving in the central cell memory.

References

The references relied on by the Examiner are as follows:

Bray	5,487,061	Jan. 23, 1996
Norizuki et al. (Norizuki)	5,570,361	Oct. 29, 1996
Kozaki et al. (Kozaki)	5,838,677	Nov. 17, 1998 (filed Apr. 15, 1996)
Des Jardins et al. (Des Jardins)	5,936,939	Aug. 10, 1999 (filed May 22, 1995)
Hatano et al. (Hatano)	5,959,991	Sep. 28, 1999 (filed Oct. 16, 1996)

Rejections at Issue

Claims 10, 11 and 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hatano in view of Des Jardins.

Claims 12, 13, 15, 21, 22 and 24 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hatano in view of Des Jardins, Norizuki and Bray.

Claim 25 stands rejected under 35 U.S.C. § 103 as being unpatentable over Hatano in view of Des Jardins and Kozaki.

Throughout the opinion, we make reference to the briefs[2] and to the answer for the respective positions of Appellants and the Examiner.

OPINION

With full consideration being given to the subject matter on appeal, the Examiner's rejections and the arguments of Appellants and the Examiner, for the reasons stated ***infra***, we reverse the Examiner's rejection of claims 10-13, 15, 20-22, 24 and 25. under 35 U.S.C. § 103.

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a ***prima facie*** case of obviousness. ***In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ 1443, 1444 (Fed Cir. 1992). See also ***In re Piasecki***, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed Cir. 1984). The Examiner can satisfy this burden by showing

[2] Appellants filed an appeal brief on June 25, 2001. Appellants filed a reply brief on October 3, 2001. The Examiner mailed out an office communication on December 19, 2001 stating that the reply had been entered.

that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. ***In re Fine***, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. ***Oetiker***, 977 F.2d at 1445, 24 USPQ at 1444. ***See also Piasecki***, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and arguments." ***In re Oetiker***, 977 F.2d at1445, 24 USPQ2d at 1444. [T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." ***In re Lee***, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). With these principles in mind, we commence review of the pertinent evidence and arguments of Appellants and the Examiner.

For the rejections of claims 10, 11 and 20 under 35 U.S.C. § 103 as being unpatentable over Hatano in view of Des Jardins, Appellants argue that neither Hatano nor Des Jardins teaches that each ATM cell of the packet containing said received cell is discarded before arriving in the central cell memory. In particular, Appellants argue

that Des Jardins teaches that the buffer is not enabled to write and thus discard occurs in the memory itself. See pages 5-7 of the brief and the reply brief.

We note that Appellants' claim 10 recites:

> comparator means cooperating with the counting means and the control logic means such that, responsive to the programmable threshold value for the degree of filling of the central cell memory being reached , and evaluation of information determinable from the header of a received cell relating to the packet of which the received cell is a part, each ATM cell of the packet containing said received cell is discarded before arriving in the central cell memory.

Similarly claim 20 recites:

> said comparator means cooperating with the counting means and the control logic means such that, responsive to a programmable threshold value for the degree of filling of the central cell memory being reached, and evaluation of information determinable from the header of a received cell relating to the packet of which the received cell is a part, a programmable number of links are defined on the basis of the sequence of arrival of the ATM cells assigned to a relevant link, each ATM cell of the packet belonging to the defined VC value being discarded before arriving in the central cell memory.

We further note that claims 10 and 20 are the only independent claims before us.

For this limitation, the Examiner relies on Des Jardins and points to column 2, lines 54-60, see pages 4 and 7 of the Examiner's answer.

Turning to Des Jardins, we find that the buffer control enables an early packet discard control arrangement in which, when the buffer instantaneously buffers a selected number of cells, it disables the buffer from buffering cells which are related to packets for which it did not begin receiving cells prior to enabling the early packet discard control arrangement mechanism. See column 2, lines 54-60 of Des Jardins. With reference to Figure 3, Des Jardins teaches that the control element 35 enables cells received from the input communication links to be buffered into the buffer 32. If the buffer 32 overflows, the control element 35 will disable the buffer 32 from buffering cells and will allow those cells to be discarded. See Des Jardins, column 5, lines 60-65.

From our reading of Des Jardins as a whole, we find that Des Jardins teaches that the data to be buffered is applied to the data lines of buffer 32. Control element 35 can discard this data by simply preventing the data that is present on the data lines in each of the memory cells to be clocked into the data cells. Thus, in the Des Jardins system, the ATM cells do arrive in the central memory cells since they are placed on the data lines of each of the memory cells of buffer 32. This is in contrast to Appellants' Figure 4 in which the data is prevented from arriving at the memory cells via gate 42. Therefore, we fail to find that Des Jardins teaches the above recited limitations of independent claims 10 and 20 and therefore we will not sustain the Examiner's rejection of claims 10, 11 and 20 under 35 U.S.C. § 103 as being unpatentable over Hatano in view of Des Jardins.

For the rejection of the dependent claims 12, 13, 15, 21, 22, 24 and 25 under 35 U.S.C. § 103, we note that the Examiner relies on Des Jardins for the above limitations of these rejections as well. Furthermore, we fail to find that the cited art supplies this missing piece. Therefore, we will not sustain these rejections for the same reasons as stated above.

In view of the foregoing, we have not sustained the Examiner's rejections of claims 10-13, 15, 20-22, 24 and 25 under 35 U.S.C. § 103.

REVERSED

LEE E. BARRETT Administrative Patent Judge	)
MICHAEL R. FLEMING Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
HOWARD B. BLANKENSHIP Administrative Patent Judge	)

MRF/vsh

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