

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KOYU YAMANOI and TAKASHI SUGASAWA

Appeal No. 2002-1594
Application No. 09/057,573

HEARD: February 20, 2003

Before HAIRSTON, RUGGIERO, and BLANKENSHIP, Administrative Patent Judges.
BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-3 and 7-9, which are all the claims remaining in the application.

We affirm-in-part.

BACKGROUND

The invention is directed to qualification of signals in an optical disc apparatus, in particular suppressing system response to any effects of DC component variation.

Claim 7 is reproduced below.

7. An apparatus for the qualification of a signal comprising:

a phase locked loop synchronizer, said phase locked loop synchronizer producing phase error signals in response to an analog signal input, said phase locked loop synchronizer further adjusting a signal slice level in response to said analog signal from a jitter feedback slicer, said jitter feedback slicer responding to said phase error signals to one of increase or decrease a voltage of said analog signal input to compensate for a change in said signal slice level from said jitter feedback slicer.

The examiner relies on the following references:

Saiki et al. (Saiki)	5,467,331	Nov. 14, 1995
Kawashima et al. (Kawashima)	5,966,356	Oct. 12, 1999 (filed Nov. 7, 1997)

Claims 1-3 and 7-9 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kawashima and Saiki.

We refer to the Final Rejection (Paper No. 11) and the Examiner's Answer (Paper No. 18) for a statement of the examiner's position and to the Brief (Paper No. 16) for appellants' position with respect to the claims which stand rejected.

OPINION

In response to the section 103 rejection of instant claim 1, appellants argue that Kawashima fails to teach the step of detecting a direction and magnitude of a slice level shift from the slicer based on at least one phase error signal. (Brief at 6.)

The examiner responds that Kawashima detects both direction and magnitude of the slice level shift, referring to “col. 2, lines 40 plus.” (Answer at 4.)

Kawashima at column 2, line 39 et seq. describes the “time chart” comprised of Figures 8(b) and 8(c), relating to the conventional apparatus shown in Figure 7. The identified section of Kawashima describes correcting slice level B upward (Fig. 8(b)) or downward (Fig. 8(c)). The correction of slice level, however, refers to generation (by generating section 16; Fig. 7), rather than detection of slice level shift. Kawashima describes detection of slice level at column 2, lines 1-25. Data detector 14 (Fig. 7) compares output A of the AGC circuit and equalizer 13 with slice level signal B, and converts output A (originating from photodetector 4A) into binary data of “0” or “1.”

We find no express disclosure of detecting a direction and magnitude of a slice level shift from a slicer based on a phase error signal, and controlling the slicer in accordance with the detection, as required by instant claim 1. Nor has the examiner set forth any reasoning with respect to why Kawashima’s detection might be recognized by the artisan as necessarily performing (i.e., under the principles of inherency) the step recited in the claim.

We thus agree with appellants that a case for prima facie obviousness of the subject matter as a whole of claim 1 has not been established. We do not sustain the rejection of claim 1, nor of claims 2 or 3 depending therefrom.

In response to the rejection of claim 7, appellants argue that Kawashima does not disclose or suggest the jitter feedback slicer responding to the phase error signals to one of increase or decrease the voltage of the analog input signal to compensate for change in the signal/slice level from the jitter feedback signal. (Brief at 6.) The examiner responds that, as depicted in Figure 2 or 4 of Kawashima “the error signal c is sent to a summing amplifier 4 [sic; 24]” where it is summed with the input from the buffer amplifiers, meeting “at least one of” an increase or decrease of the analog input signal as claimed. (Answer at 5.)

Figure 2 of Kawashima is a circuit diagram of an embodiment of a slice level generating section wherein peak detection and bottom detection section 30 and slice level generating section 32 (Fig. 1) are combined. Col. 7, ll. 1-6. Summing amplifier 24 receives on one input the output of buffer amplifier 23 and on the other input error signal C from phase comparator 15, thus summing the signals and generating slice level B. Col. 7, ll. 26-33.

We agree with the examiner that Kawashima teaches the limitations of claim 7 that appellants argue in the Brief as being absent from the reference. Counsel for appellants agreed with the examiner’s assessment, thus conceding the point, at the oral hearing. We do not find the argument in the Brief persuasive of nonobviousness.

The only other argument in the Brief relevant to claim 7 and the rejection of record is the allegation that “Saiki is not a slicer and consequently could not be used to reject the present claimed invention.” (Brief at 7.)

The rejection does not rely on Saiki as disclosing a slicer, and thus whether or not Saiki is a “slicer” is irrelevant. Appellants’ argument may, however, be read as faulting the examiner’s finding of motivation to combine the references.¹

The examiner finds that Kawashima discloses all of claim 7 except that phase comparator 15 (col. 5, ll. 37-42; Fig. 1) lacks phase locked loop capability. Saiki discloses the well known advantages (e.g., col. 7, ll. 1-12) of phase locked loop circuitry and thus the suggestion for combination with Kawashima. We therefore consider the examiner’s finding of motivation to make the proposed combination to be supported by the evidence of record.

We are thus not persuaded that the conclusion of prima facie obviousness of the subject matter as a whole of claim 7 is erroneous. Since appellants provide no arguments for separate patentability of the dependent claims, we sustain the section 103 rejection of claims 7-9. See 37 CFR § 1.192(c)(7).

We have considered all of appellants’ arguments in making our determinations. Arguments not relied upon are deemed waived. See 37 CFR § 1.192(a) (“Any

¹ The presence or absence of a motivation to combine references in an obviousness determination is a pure question of fact. In re Gartside, 203 F.3d 1305, 1316, 53 USPQ2d 1769, 1776 (Fed. Cir. 2000).

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arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences, unless good cause is shown”) and § 1.192(c)(8)(iv) (the brief must point out the errors in the rejection).

CONCLUSION

The rejection of claims 1-3 under 35 U.S.C. § 103 is reversed, but the rejection of claims 7-9 is affirmed. The examiner’s decision in rejecting claims 1-3 and 7-9 is thus affirmed-in-part.

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No time period for taking any subsequent action in connection with this appeal
may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH F. RUGGIERO)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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HOWARD B. BLANKENSHIP)	
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