

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TERRY LEE LEASURE, GEORGE McNEIL LATTIMORE,
ROBERT ANTHONY ROSS, Jr. and GUS WAI YAN YEUNG

Appeal No. 2002-1994
Application No. 09/364,449¹

ON BRIEF

Before THOMAS, BLANKENSHIP and SAADAT, Administrative Patent Judges.

SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 4-8, 11, 14, 15, 17 and 18. Claims 1-3 and 10 have been canceled. Claims 9, 12, 13, 16, 19-29, which are all the other claims pending in this application, are indicated by the Examiner as being allowable.²

We affirm.

¹ Application for patent filed July 30, 1999.

² See the Examiner's answer, pages 2 and 9.

BACKGROUND

Appellants' invention relates generally to an apparatus for cache reads, and more specifically, to unaligned reads from a cache having a fixed alignment of bytes on a fixed alignment boundary. According to Appellants, to perform a read in which the first data value does not correspond to the cache boundary, an entire cache line is accessed (specification, page 2). Next, the unused bytes, which remain after an unaligned double word byte sequence is extracted are effectively thrown away (id.).

Representative claims 4, 6 and 17 are reproduced bellow:

4. An apparatus for cache read operations comprising:

a cache line having a plurality of storage units wherein each storage unit is operable for storing a data signal from a bus operable for communicating a plurality of data signals, and wherein a first sequence of said plurality of data signals is remapped into a second sequence of data signals in said plurality of storage units wherein said plurality of storage units further comprises a plurality of groups of storage units, and wherein each group of the plurality of groups is operable for reading a data value from a corresponding storage unit in said group.

6. The apparatus of claim 5 wherein said circuitry comprises:

a logic array operable for receiving an address and outputting a signal operable for selecting said data value.

17. A method of unaligned cache read operations comprising the steps of:

remapping a plurality of data signals for storage into a cache line including a plurality of storage units;

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selecting a subset of said plurality of storage units for reading in response to an address therefor.

The Examiner relies on the following reference in rejecting the claims:

Thatcher et al. (Thatcher) 6,085,289 Jul. 4, 2000
(filed Jul. 18, 1997)

Claims 4-8, 11, 14, 15, 17 and 18 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Thatcher.

We make reference to the answer (Paper No. 9, mailed April 17, 2002) for the Examiner's reasoning and to the brief (Paper No. 8, filed February 11, 2002) and the reply brief (Paper No. 10, filed June 24, 2002) for Appellants' arguments thereagainst.

OPINION

At the outset, we note that Appellants indicate that claims 4, 5 and 8 constitute one group, claims 6 and 7 stand or fall together, claims 17 and 18 stand or fall with one another, while claims 11, 14 and 15 stand or fall together (brief, page 8). We observe that Appellants have, in the arguments section of the brief, provided separate arguments for each group, as required by 37 CFR § 1.192(c)(7) (July 1, 2000). Therefore, we will consider Appellants' claims as standing or falling together as argued in the brief and limit our consideration to claims 4, 6,

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11 and 17 as the representative claims of their corresponding groups.

With respect to the rejection of claim 4, the focus of Appellants' arguments is that reading the claimed plurality of storage units as "bits" in Thatcher and reading the recited plurality of groups as Thatcher's "words" is improper (brief, page 8). Appellants point out that the claimed "groups" refer to the storage units having remapped data whereas a word refers to a multi-byte entity having a particular arrangement (id.). Appellants further argue that equating a storage unit with the "bit" of Thatcher in view of the bit organization disclosed in the reference (col. 3, lines 27-48) does not result in storage units corresponding to a group but, to the words being read (brief, pages 9 & 10).

In response to Appellants' arguments, the Examiner points out that the main issue contended by Appellants is whether each group of the plurality of groups is operable for reading a data value from a corresponding storage unit in the group (answer, page 7). The Examiner argues that the original 8 words in the cache line are interleaved among each other such that their bits are intermixed with bits from all the other words (answer, page 7). The Examiner further asserts that the rearrangement of the

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original cache line allows Thatcher to perform the desired formatting so that groups of bits are output from the remapped cache line (id.).

A rejection for anticipation under section 102 requires that the four corners of a single prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. See Atlas Powder Co. v. Ireco Inc., 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999); In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994). The inquiry as to whether a reference anticipates a claim must focus on what subject matter is encompassed by the claim and what subject matter is described by the reference. As set forth by the court in Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983), it is only necessary for the claims to "'read on' something disclosed in the reference, i.e., all limitations of the claim are found in the reference, or 'fully met' by it." Furthermore, anticipation requires a finding that the claim at issue "reads on" a prior art reference. See also Atlas Powder Co. v. IRECO Inc., 190 F.3d at 1346, 51 USPQ2d at

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1945 (Fed. Cir. 1999) (quoting Titanium Metals Corp. v. Banner, 778 F.2d 775, 781, 227 USPQ 773, 778 (Fed. Cir. 1985)).

After reviewing Thatcher, we find that the Examiner presents sufficient evidentiary support to establish a prima facie case of anticipation. We disagree with Appellants' argument that the claimed plurality of storage units and groups is not the same as Thatcher's bits and words because a word is a unit of information constituting a consecutive sequence (brief, page 9). Even if Appellants' assertion is correct, claim 4 does not preclude a consecutive sequence for the storage units within groups of storage units because the claim merely requires a plurality of storage units which further comprises a plurality of groups of storage units for storing data signals. Therefore, the claimed "remapping" of data signals in a second sequence of data signals in the plurality of storage units also reads on organizing a cache line of Thatcher (col. 1, lines 55-60) which is performed by:

[G]rouping each corresponding bit of each byte in a cache line of data together, and expanding the grouping with an organization formed by one bit from a same byte within each word.

We also find that, contrary to Appellants' position (reply brief, page 2), the Examiner has correctly characterized the claimed "reading a data value from a corresponding storage unit

in said group" as bit selection of Thatcher. The Examiner's position with regard to the reading of the stored data in its reorganized format and the benefits of remapping of Thatcher (answer, page 8), is supported by the reference teaching wherein the selection of bit 0 of byte 31 requires traveling across only 32 bits instead of the entire cache line 256 bits (col. 5, lines 10-25).

Additionally, we remain unconvinced by Appellants' argument (brief, page 9) that the claimed "each group of the plurality of groups is operable for reading a data value from a corresponding storage unit is said group" does not read on the organization of bytes in Thatcher (grouping all the bit 0s of each byte together, all of the bit 1s of each byte together, etc.) (Col. 3, lines 27-48). In fact, Thatcher does show that each group (word) is operable for reading a data value from a corresponding storage unit (bit) in said group, which is disclosed as the specific scheme of data selection requiring minimal wiring (col. 3, lines 49-60). We also note that the organization of data based on interleaving bytes of the bus, similar to data organization of Thatcher, is described in Appellants' specification in support of the claims wherein lines for byte 0 are coupled to the 0 byte of cache group 0, lines for byte 01 is

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coupled to byte 0 of cache group 01, and so forth
(specification, page 11, lines 17-21).

In view of the analysis above, we find that the examiner has met the burden of providing a prima facie case of anticipation by showing that Thatcher teaches a plurality of storage units and a plurality of groups of storage units wherein "each group of the plurality of groups is operable for reading a data value from a corresponding storage unit is said group", as recited in independent claim 4. Accordingly, we sustain the 35 U.S.C. § 102 rejection of claim 4, as well as claims 5 and 8 which are grouped with claim 4 as standing or falling therewith, over Thatcher.

Turning now to the rejection of claim 6, as well as claim 7 which is grouped therewith, Appellants assert that the control mechanism of Thatcher is not disclosed to be a logic array (brief, page 11). The Examiner responds by relying on Figures 1 and 2 of Thatcher and asserts that the data formatter includes an array of logic which receives the formatter address for selecting the data value in a storage unit (answer, page 9). We also find that Thatcher discloses circuitry for selecting a data value including an address generator 10 for providing the formatter address to the data formatter 14 which is used to

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access a data value from the units in the cache line (col. 2, lines 53-61). Although Thatcher does not particularly mention using a logic array, a series of circuitry including logic gates, as shown in Figure 2, is used for addressing the cache line and retrieving data values based on the provided address. Therefore we agree with the Examiner that the claimed "logic array" reads on the circuitry disclosed by Thatcher for selecting a cache line and reading the data value stored therein based on its address since the claim does not require any particular type of logic array. Accordingly, the 35 U.S.C. § 102 rejection of claims 6 and 7 is sustained.

With respect to claim 11, Appellants provide the same arguments as those provided for claim 4 (brief, page 12). For the same reasons discussed above with respect to claim 4, we sustain the 35 U.S.C. § 102 rejection of claim 11, as well as claims 14 and 15 which are grouped therewith, over Thatcher.

Turning now to claim 17, Appellants argue that the claimed "selecting a subset of said plurality of storage units" is not taught by Thatcher (brief, page 13). In response, the Examiner asserts that Thatcher does select a subset of the plurality of storage units for output to the CPU regardless of the fact that the entire line may be input to the formatter (answer, page 9).

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We note that the claim merely requires that a subset of the plurality of the storage units be selected and eventually read. Therefore, the Examiner has reasonably relied on Figure 2 of Thatcher since the data from the cache line is straight forward muxed into the selection device 24 which in turn, selects a subset of the plurality of the storage units for even and odd selectors 26 and 28 (col. 3, lines 61-67). Accordingly, claim 17 reads on the prior art reference and its anticipation rejection over Thatcher, as well as that of claim 18 which is grouped therewith, is sustained.

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CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 4-8, 11, 14, 15, 17 and 18 under 35 U.S.C. § 102 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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HOWARD B. BLANKENSHIP)	APPEALS
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