

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte TOSHIYUKI NAGATA, HIROYUKI YOSHIDA,  
MASAYUKI MOROI and ATSUSHI SATOH

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Appeal No. 2002-2072  
Application No. 09/332,360

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ON BRIEF

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Before KRASS, FLEMING and JERRY SMITH, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1, 3 and 4.

The invention is directed to a random access memory, best illustrated by reference to representative independent claim 1, reproduced as follows:

Appeal No. 2002-2072  
Application No. 09/332,360

1. A random access memory, comprising:

an array of capacitors, ones of said capacitors being electrically coupled by a conductive plate which overlies said array of capacitors wherein the pattern of said conductive plate is continuous in at most one dimension, but not in two dimensions; and

the conductive plate is patterned in strips which are diagonal to gate structures underlying said array.

The examiner relies on the following reference:

|       |           |                                       |
|-------|-----------|---------------------------------------|
| Chang | 6,020,235 | Feb. 1, 2000<br>(filed Apr. 14, 1998) |
|-------|-----------|---------------------------------------|

Claim 1 stands rejected under 35 U.S.C. § 102(e) as anticipated by Chang.

Claims 3 and 4 stand rejected under 35 U.S.C. § 103 as unpatentable over Chang.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

#### OPINION

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed.

Appeal No. 2002-2072  
Application No. 09/332,360

Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

In the instant case, with regard to claim 1, the examiner contends that Chang discloses the claimed subject matter because core 14 of Chang is a conductive plate (column 3, lines 4-5: the core can form "a part of the upper electrode") overlying an array of capacitors, and, as shown in Chang's Figure 3, the pattern of conductive plates 14 is continuous in at most one directed but not in two dimensions and these plates are strips which are diagonal to the gate structures.

Appellants disagree with the examiner's analysis only in the allegation that core 14 of Chang overlies an array of capacitors. It is appellants' position that since core 14 comprises part of the bottom electrode of the capacitor structure in Chang, "it is physically impossible for the core (14) to both form the bottom electrode of the capacitor and overlies the capacitor as required by claim 1..." (Brief-page 3).

We disagree. As explained by the examiner, at pages 6-7 of the answer, Chang's core 14 not only comprises part of the bottom electrode, but is also "a part of [the] top electrode of [the] capacitor structure. The core (14) overlies the bottom

Appeal No. 2002-2072  
Application No. 09/332,360

electrodes (polysilicon layers 13 of bottom electrodes) of array capacitors." While it may, initially, seem awkward to say that an element which forms the bottom electrode may overlie the capacitor array, when we review the instant disclosure, it appears that this is just what appellants disclose. For example, in Figure 8 of the instant application, it appears that conductive plate layer 120, which forms part of the capacitors 130, also serves to overlie the capacitors. It appears to us that appellants would be hard pressed to argue that it is impossible for a conductive layer to form part of an electrode of a capacitor and overlie that capacitor at the same time when it appears that this is the way appellants' own conductive layer is formed.

We will sustain the rejection of claim 1 under 35 U.S.C. 102(e).

With regard to claim 3, the examiner contends that it "is known in the art that the upper plates of the capacitors in DRAM are commonly used to connect together as a common plate in order to provide the same applied voltage to the memory cells in the array" (answer-page 4).

Appellants only response is to deny the examiner's allegation and to challenge the examiner to provide relevant art

Appeal No. 2002-2072  
Application No. 09/332,360

to support the examiner's allegation. The examiner has done just that, citing U.S. Patent Nos. 5,640,030, 5,682,344, 5,341,326 and 5,805,495.

The burden now shifted to appellants to show, by argument, or objective evidence, why the cited references do not show what the examiner alleges they show. Since appellants have not responded to the examiner's showing, we will sustain the examiner's rejection of claim 3 under 35 U.S.C. § 103.

Finally, turning to claim 4, it is the examiner's position that Chang discloses a bitline connected to a bitline contact but that Figure 3 did not explicitly show the bitline overlying a plurality of transistors and that the conductive plate is patterned so that it does not affect alignment relationships in the connections between the bitline and the transistors.

The examiner alleges that since the bitline contact is clearly located between the conductive strips in Figure 3 of Chang, the formation of the conductive plates "inherently does not affect alignment relationship in the connections between the bitline and the transistors" and that "the bitline is formed overlying the transistors is well known and conventional in the art" (answer-page 5).

Appeal No. 2002-2072  
Application No. 09/332,360

Since Chang only shows a bitline contact, but does not show the bitlines themselves, nor does Chang discuss any relationship between bitlines and transistors, in our view, the examiner's rationale is no more than speculation. We cannot say, from Chang's disclosure, that there is a bitline overlying a plurality of transistors nor can we say that the conductive plate 14 is patterned such that it "does not affect alignment relationships in said connections between said bitline and said transistors," as claimed.

Accordingly, we will not sustain the rejection of claim 4 under 35 U.S.C. § 103.

Since we have sustained the rejection of claims 1 and 3 but we have not sustained the rejection of claim 4, the examiner's decision is affirmed-in-part.

Appeal No. 2002-2072  
Application No. 09/332,360

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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|-----------------------------|---|-----------------|
| ERROL A. KRASS              | ) |                 |
| Administrative Patent Judge | ) |                 |
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|                             | ) |                 |
| MICHAEL R. FLEMING          | ) | BOARD OF PATENT |
| Administrative Patent Judge | ) | APPEALS AND     |
|                             | ) | INTERFERENCES   |
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|                             | ) |                 |
| JERRY SMITH                 | ) |                 |
| Administrative Patent Judge | ) |                 |

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Appeal No. 2002-2072  
Application No. 09/332,360

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