The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte DUSAN PETRANOVIC, RANKO SCEPANOVIC, and IVAN PAVISIC

Appeal No. 2002-2086
Application 09/010,396[1]

ON BRIEF

Before BARRETT, DIXON, and BARRY, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1, 6-8, 12, 18, and 22-26. Claims 2, 4, 9, 11, 13, 15, 19, and 21 are allowed. Claims 3, 5, 10, 14, 16, 17, 20, 27-30 have been canceled.

We affirm-in-part.

[1] Application for patent filed January 21, 1998, entitled "Timing-Driven Placement Method Utilizing Novel Interconnect Delay Model."

BACKGROUND

The invention relates to calculation of the interconnect delay between the driver and one of the sinks on a net in an integrated circuit.

Claim 1 is reproduced below.

> 1. A method for placement of a plurality of cells on a surface of an integrated circuit, said method comprising the steps of:
>
> calculating an interconnect delay, defined as a delay for an interconnect between a driver and a sink in a placement of cells;
>
> comparing the placement of cells to predetermined cost criteria which include a timing criterion based upon the interconnect delay; and
>
> moving cells in the placement of cells to alternate locations on the surface if necessary to satisfy the predetermined cost criteria,
>
> wherein the interconnect is part of a net, and wherein calculation of the interconnect delay comprises determining a first delay that accounts for a contribution of a direct path between the driver and the sink and determining a second delay that accounts for a contribution of a portion of the net that does not include the direct path to the interconnect delay.

The examiner relies on the following reference:

Li et al. (Li)	5,666,290	September 9, 1997

Claims 1, 6-8, 12, 18, and 22-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Li.

We refer to the final rejection (Paper No. 13) (pages referred to as "FR__") and the examiner's answer (Paper No. 19)

(pages referred to as "EA__") for a statement of the examiner's rejection, and to the brief (Paper No. 18) (pages referred to as "Br__") for a statement of appellants' arguments thereagainst.

OPINION

Note

It appears that the upper bound on the summation in equation (9) (specification, p. 8) should be "k" instead of "i".

Group 1 - claims 1, 6-8, 12, 18, and 22

The issue is whether Li discloses or suggests "calculating an interconnect delay, defined as a delay for an interconnect between a driver and a sink in a placement of cells; ... wherein the interconnect is part of a net, and wherein calculation of the interconnect delay comprises determining a first delay that accounts for a contribution of a direct path between the driver and the sink and determining a second delay that accounts for a contribution of a portion of the net that does not include the direct path to the interconnect delay" (claim 1). Independent claims 5, 12, and 18 have a similar limitation.

The examiner relies on the following statements in Li:

> Once the overall length of the nets coupled to a segment has been estimated, the delay through each critical path is calculated by summing the delays for the individual segments making up each critical path. [Col. 10, line 66 to col. 11, line 2.]

> The interconnect delay constituents for each segment of a critical path are then summed and added to those delay constituents which are intrinsic to the components of each segment within the critical path to calculate the overall current delay for the critical path D_r. [Col. 11, lines 62-66.]

See claim charts at EA4, EA5. The examiner also refers (at EA7) to Li, column 6, lines 30-50.

Appellants argue that none of the terms involved in the calculation of the segment delay D_S discloses or remotely suggests the present invention's feature of calculating an interconnect delay by determining a first delay that accounts for a contribution of a direct path between a driver and a sink and determining a second delay that accounts for a contribution of a portion of the net that does not include the direct path to the interconnect delay (Br9).

The examiner's discussion of appellants' arguments in the Response to Final Rejection (Paper No. 13) (EA6-7) indicates an understanding of the invention. The examiner maintains that Li at least suggests the invention (EA7). The examiner refers to Fig. 9 of Li and finds that "[c]alculating the delay along one segment of the critical path of net 112, e.g. from node 110 to node 116, requires consideration of the delay contributions from the other two branches of net 112, specifically, from node 110 to node 124 and node 110 to node 122" (EA7-8).

The examiner does not explain the basis for finding that calculating the delay from driver pin 110 to sink 116 requires

consideration of the delay contributions from driver pin 110 to sink 124 and from driver pin 110 to sink 122. The examiner's reliance on the calculation of interconnect delay for the critical path of Li does not support the finding. The critical path is a single path through the circuit, e.g., part of the critical path could be "between driver pin 108 and input pin 116 [in Fig. 9]" (col. 11, lines 56-57). Li states (col. 6, lines 30-34):

> The path delay is calculated by determining the sum of the delays D_S through each segment of the path. A segment typically includes one of the components of the circuit and the net which couples an output of the component to one or more inputs of components.

The segments are along the critical path, e.g., from driver 108 to sink 116 in Fig. 9, and do not include the delay of non-critical path segments, e.g., from driver 108 to sink 122 or sink 124, as stated by the examiner.

Nevertheless, the broad language of the claims appears to read on Li. We look at the delays for one segment, i.e., between two components, explained at column 2, lines 34-61, and column 6, lines 39-50; this delay is the claimed "interconnect delay, defined as a delay for an interconnect between a driver and a sink in a placement of cells." The segment delay D_S is for the segment in the critical path, e.g., from driver 108 to sink 116. The limitation of "a first delay that accounts for a contribution of a direct path between the driver and the sink" appears to read

on the delay D_{RC}, where "D_{RC} is the propagation delay of a signal along the branch of the net of the segment which couples the output of the component of the segment to the input of the component of the next segment of the critical path" (col. 6, lines 45-49). The limitation of "a second delay that accounts for a contribution of a portion of the net that does not include the direct path to the interconnect delay" appears to read on the delay $S \cdot C_{in}$ where "S is the effective resistance of the component, C_{in} is the total capacitance of all inputs to which the net of the segment is coupled" (col. 6, lines 42-44) because this delay accounts for contributions of capacitances of the net that are not in a direct path from source to sink. To the extent $S \cdot C_{in}$ includes the capacitance of the sink and might be considered part of the "first delay," this is merely a matter of grouping terms. The limitation "wherein calculation of the interconnect delay comprises" does not exclude other delay terms. Absent some explanation by appellants as to why this interpretation of the claims is not reasonable, we sustain the rejection of claims 1, 6-8, 12, 18, and 22.

<u>Group 2 - claims 23-26</u>

These dependent claims recite "wherein modeling the interconnect comprises utilizing a term that corresponds to a length of an overlapping wire."

The examiner refers to appellants' specification which states that "l_{oji} is length of the overlapping wire that connects driver and sinks j and i" (spec. at 8) and states that "[a]ppellants do not provide or attach any particular meaning to the term 'overlapping wire' which would ordinarily mean one wire crossing another" (EA9). The "[e]xaminer asserts that a segment that crosses a cut line is an overlapping segment and further asserts that an algorithm that is attempting to minimize the weight of all net segments crossing the cut line must necessarily include a term that accounts for the net segment" (EA10).

Appellants argue that nothing in Li indicates that Li's min-cut algorithm automatically accounts for overlapping wires or even that Li's min-cut algorithm is used in the calculation of an interconnect delay between a driver and a sink (EA10).

It appears that the examiner is relying on the term "overlapping wire" being undefined and therefore being so broad that it is met by anything. If a term is considered indefinite, the claims should be rejected under 35 U.S.C. § 112, second paragraph. In this case, while it would have been desirable to have a definition in the specification, we consider that "overlapping wire" has a known meaning in the interconnect delay and refers to the portion of the unique path between the input and node "i" that is common with the unique path between the input and node "k". See R. Gupta and L.T. Pileggi, The Elmore

Delay as a Bound for RC Trees with Generalized Input Signals, IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol 16, No. 1, January 1997, p. 96 (discussing R_{ki}); L. van Ginneken, Buffer Placement in Distributed RC-tree Networks for Minimal Elmore Delay, IEEE Int'l Symposium on Circuits and Systems, Vol. 2, May 1990, p. 866 (discussing R_{ki}) (both references of record). If this is not the meaning intended by appellants, it must be shown what meaning would be given by one of ordinary skill in the art. The min-cut algorithm of Li has nothing whatsoever to do with overlapping wires even under the examiner's interpretation. Accordingly, we conclude that the examiner has failed to establish a prima facie case of obviousness. The rejection of claims 23-26 is reversed.

Requirement

In any further prosecution, either by request for rehearing or by further prosecution before the examiner, in addition to explaining how the claims define over Li, appellants are required to explain how the limitations, "wherein calculation of the interconnect delay comprises determining a first delay that accounts for a contribution of a direct path between the driver and the sink and determining a second delay that accounts for a contribution of a portion of the net that does not include the direct path to the interconnect delay" (claim 1) and "wherein

modeling the interconnect comprises utilizing a term that corresponds to a length of an overlapping wire" (claim 23), distinguish over the delay expression $D_i = \sum R_{ki}C_k$ (summation over all k) in van Ginneken and $T_{Di} = \sum R_{ki}C_k$ (summation over all k) in Gupta (cited above). The expansion of each of these summations can be partitioned into one term representing delay from a direct path and a second summation representing a delay which accounts for a contribution of the net that does not include the direct path, e.g., using Gupta:

$$D_i = D_{LINKi} + D_{TPLGi} = R_{ii}C_k + \sum_{k \neq i} R_{ki}C_k$$

Where D_i, D_{LINKi}, and D_{TPLGi} correspond to Δ_{INTi}, Δ_{LINKi}, and Δ_{TPLGi}, respectively, in equations (7)-(9) on page 8 of appellants' specification, except that there is no unit length capacitance c_0 and the resistance is a lump resistance R_{ki} rather than a function of length $r_0 l_{oji}$. Since no equation or model (e.g., a unit length capacitance) is claimed, the limitations of first and second delays do not appear to distinguish over the delay expressions in these two references. Both expressions also involve overlapping wires as recited in claim 23.

CONCLUSION

The rejection of claims 1, 6-8, 12, 18, and 22 is sustained.

The rejection of claims 23-26 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

LEE E. BARRETT Administrative Patent Judge	)	
JOSEPH L. DIXON Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

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