

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte MUTSUHIRO OHMORI and TOSHIO HORIOKA

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Appeal No. 2003-0796  
Application No. 09/260,031<sup>1</sup>

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HEARD: APRIL 13, 2004

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Before GROSS, BARRY, and SAADAT, Administrative Patent Judges.  
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 6-15. Claims 1-5 have been canceled.

We reverse.

BACKGROUND

Appellants' invention is directed to a graphic drawing image processing apparatus including a memory circuit for storing display data and texture data required by one or more graphic elements. A logic circuit is also included which performs the

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<sup>1</sup> Application for patent filed March 2, 1999, which claims the foreign filing priority benefit under 35 U.S.C. § 119 of Japanese Applications No. P10-052017, filed March 4, 1998 and No. P11-016529, filed January 26, 1999.

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processing for applying the texture data on the surface of the graphic element based on the stored data.

Representative independent claim 6 is reproduced below:

6. An image processing apparatus for performing rendering by receiving polygon rendering data including three-dimensional coordinates  $(x, y, z)$ , R (red), G (green), and B (blue), homogeneous coordinates  $(s, t)$  of a texture, and a homogeneous term  $q$  with respect to vertexes of a unit graphic, said image processing apparatus comprising:

a memory circuit for storing display data and texture data required by at least one graphic element;

an interpolation data generation circuit for interpolating the polygon rendering data of vertexes of the unit graphic to generate interpolation data of pixels positioned inside the unit graphic; and

a texture processing circuit for dividing the homogeneous coordinates  $(s, t)$  of a texture included in the interpolation data by the homogeneous term  $q$  to generate " $s/q$ " and " $t/q$ ", using a texture address corresponding to the " $s/q$ " and " $t/q$ " to read texture data from the memory circuit, and applying the texture data on the surface of the graphic element of the display data;

the memory circuit, the interpolation data generation circuit, and the texture processing circuit being accommodated in one semiconductor chip.

The Examiner relies on the following references in rejecting the claims:

Hannah et al. (Hannah)	5,706,481	Jan. 6, 1998
Coelho	6,107,987	Aug. 22, 2000
	(effectively filed Apr. 29, 1994)	

Foley et al. (Foley), "Computer Graphics, Principles and Practice," Second edition, Addison-Wesley, 1997, pp. 204-205.

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Claims 6-8, 10-13 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hannah in view of Foley.

Claims 9 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hannah in view of Coelho.<sup>2</sup>

We make reference to the final rejection (Paper No. 12, mailed August 10, 2001) and the answer (Paper No. 15, mailed January 15, 2002) for the Examiner's reasoning, and to the appeal brief (Paper No. 14, filed November 13, 2001) and the reply brief (Paper No. 17, filed March 14, 2002) for Appellants' arguments thereagainst.

#### OPINION

With respect to the rejection of claims 6-8, 10-13 and 15, Appellants acknowledge that Hannah discloses a texture processing circuit on a chip while Foley discloses a division function related to homogeneous coordinates and transformations (brief, page 8). Appellants, however, argue that the claimed "texture processing circuit for dividing the homogeneous coordinates (s,t) of a texture included in the interpolation data by the homogeneous term q" is shown in neither Hannah nor Foley (brief, pages 9 & 10 and reply brief, page 3). Additionally, Appellants indicate that the transformation taught by Foley is not a circuit

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<sup>2</sup> The rejection should have probably been over Hannah and Foley in view of Coelho as the base claims are rejected over both Hannah and Foley.

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and does not generate any interpolation data to be used by a texture processing circuit in dividing the coordinates of a texture included in that interpolation data (brief, page 10 and oral hearing).

In response, the Examiner asserts that "mathematical circuitry for performing mathematical functions in the texture processing circuit" is disclosed by Hannah (answer, page 4). The Examiner further reasons that modifying the mathematical circuitry of Hannah to perform various mathematical functions other than addition would have been obvious (id.).

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). To reach a conclusion of obviousness under § 103, the examiner must produce a factual basis supported by teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Such evidence is required in order to establish a prima facie case. In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). However, "the Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed

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to support the agency's conclusion." In re Lee, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

Our review of Hannah confirms that the reference relates to an apparatus and a method for performing texture mapping in which one or more interpolators produce outputs to be displayed (col. 2, lines 40-53). Foley on the other hand merely refers to subroutine packages and processes that work with homogeneous coordinates and transformation and, as argued by Appellants (brief, pages 8 & 9), is not related to graphical displaying of textured images or texture coordinates included in interpolated data. We also agree with Appellants (reply brief, pages 2 & 3) that the interpolator of Hannah performs resampling (col. 5, lines 14-16) and addition or averaging (col. 7, lines 24-29), but not division of the coordinates included in the interpolation data by the homogeneous term  $q$ . In fact, the Examiner's position that Hannah's interpolator could be used for dividing the homogeneous coordinates of a texture is, at best, speculative since there is no teaching or suggestion in the reference to support a division using the homogeneous coordinates  $(s,t)$  and the homogeneous term  $q$ , as recited in claim 6.

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Thus, assuming, arguendo, that it would have been obvious to combine Hannah with Foley, as held by the Examiner, the combination would still fall short of teaching a texture processing circuit for dividing the homogeneous coordinates (s,t) of a texture included in the interpolation data by the homogeneous term q. We note that, similar to claim 6, independent claim 11 recites an interpolation data generation circuit and a texture processing circuit. Therefore, as the Examiner has failed to set forth a prima facie case of obviousness, we cannot sustain the 35 U.S.C. § 103 rejection of claims 6 and 11 as well as claims 7, 8, 10, 12, 13 and 15, dependent thereon, over Hannah and Foley.

With respect to the rejection of claims 9 and 14, the Examiner further relies on Coelho for teaching look-up tables coupled to a computer memory (final, page 4). However, Coelho provides no teaching related to the claimed division using the homogeneous coordinates (s,t) and the homogeneous term q and fails to overcome the deficiencies of Hannah and Foley as discussed above. Therefore, the 35 U.S.C. § 103 rejection of claims 9 and 14 cannot be sustained.

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CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 6-15 under 35 U.S.C. § 103 is reversed.

REVERSED

ANITA PELLMAN GROSS	)	
Administrative Patent Judge	)	
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	)	
	)	BOARD OF PATENT
LANCE LEONARD BARRY	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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MAHSHID D. SAADAT	)	
Administrative Patent Judge	)	

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