

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 12

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HOICHI CHEONG and HUNG QUI LE

Appeal No. 2003-0902
Application No. 09/332,413

ON BRIEF

Before SMITH, FLEMING, and MCDONALD, ***Administrative Patent Judges***.

MCDONALD, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 3, 5, 6, 9, 12, 14, 15, and 18-20. Claims 8, 17, and 21 have been indicated as allowable.

Invention

Appellants' invention relates to a system and method that groups instructions that are being dispatched for execution in a manner that enables the executing processor to restore to an operating state associated with the instruction group whenever an interruption occurs during processing of the particular

instruction group (specification, page 5, lines 20-33).

Following the fetching of multiple instructions, the fetched instructions are divided into and dispatched as groups, with each group having a first or last instruction that is an interruptible instruction (Figures 3, 7, and 9).

Claims 3 and 5 are representative of the claimed invention and are reproduced as follows:

3. A method of increasing the efficiency of execution of a processor, comprising:

dispatching instructions in instruction groups, wherein if an instruction group contains an interruptible instruction of a selected type, only one interruptible instruction of said selected type is included in said instruction group, wherein said interruptible instruction of said selected type is dispatched at the front of said instruction group;

recording a state for the processor associated with a dispatched instruction group; and

restoring said processor to said recorded state associated with said dispatched instruction group containing said interruptible instruction of said selected type causing an interrupt, in response to said interrupt from one of said interruptible instructions of said selected type.

5. A method of increasing the efficiency of execution of a processor comprising:

searching a group of N fetched instructions for an interruptible instruction of said selected type;

dispatching said group of N fetched instructions in response to not finding said interruptible instruction of said selected type in said group of N fetched instructions;

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selectively dispatching instructions from said group of instructions up to and including said interruptible instruction of said selected type, in response to finding an interruptible instruction of said selected type in said group of N fetched instructions, wherein if an instruction group contains an interruptible instruction of a selected type, only one interruptible instruction of said selected type is included in said instruction group;

recording a state for the processor associated with a dispatched instruction group; and

restoring said processor to said recorded state associated with said dispatched instruction group containing said interruptible instruction of said selected type causing an interrupt, in response to said interrupt from one of said interruptible instructions of said selected type.

References

The references relied on by the Examiner are as follows:

Peleg et al (Peleg)	5,381,533	Jan. 10, 1995
Shen et al (Shen)	5,649,136	Jul. 15, 1997
Blandy et al (Blandy)	5,940,618	Aug. 17, 1999

Rejections At Issue

Claims 5, 6, 14, 15, and 20 stand rejected under 35 U.S.C. § 103 as being obvious over the combination of Shen and Peleg.

Claims 3, 9, 12, 18 and 19 stand rejected under 35 U.S.C. § 103 as being obvious over the combination of Shen and Peleg and Blandy.

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Throughout our opinion, we make references to the Appellants' briefs, and to the Examiner's Answer for the respective details thereof.¹

OPINION

With full consideration being given to the subject matter on appeal, the Examiner's rejections and the arguments of the Appellant and the Examiner, for the reasons stated *infra*, we reverse the Examiner's rejection of claims 3, 5, 6, 9, 12, 14, 15, and 18-20 under 35 U.S.C. § 103.

I. Whether the Rejection of Claims 5, 6, 14, 15, and 20 Under 35 U.S.C. § 103 is proper?

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claim 5. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). *See also In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can

¹Appellants' filed an appeal brief on July 2, 2002. The Examiner mailed out an Office communication on August 27, 2002.

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satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. ***In re Fine***, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. ***Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444. ***See also Piasecki***, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." ***Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." ***In re Lee***, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

With respect to independent claim 5, Appellants argue that "[t]here is no motivation in either reference to combine Shen with Peleg." (brief, page 4, lines 8-9). The Examiner's position is that "Shen does not disclose that an instruction group contains only one interruptible instruction." (answer at

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page 6, lines 11-12). However, Peleg clearly discloses this feature (answer, page 6, lines 12-24). The Examiner then indicates that one of ordinary skill in the art would have recognized the advantages of incorporating the grouping of instructions into groups that contain only one interruptible instruction (answer, page 6, line 26, through page 7, line 10). We have reviewed the record before us and we agree with the Appellants. Peleg teaches the features noted above. However, so does Shen. Shen teaches at column 15, lines 39-43, that instructions are fetched in blocks for each cycle, at column 8, lines 24-36, that all interruptible instructions are checkpointed, and at column 50, lines 15-16, that instruction issue rules are used to limit the checkpointing to one instruction per cycle. Since Shen already implements "an instruction group containing only one interruptible instruction," the Examiner's stated motivation to combine the references is unpersuasive. Additionally, claim 5 requires that the interruptible instructions be at the end of the instruction block (claim 5, line 6, "up to and including"). The Examiner has provided no motivation in the rejection as to why one skilled in the art would be motivated to incorporate this feature found in Peleg into the system of Shen. Therefore, Appellants' arguments

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are persuasive and we will not sustain the Examiner's rejection under 35 U.S.C. § 103.

II. Whether the Rejection of Claims 3, 9, 12, 18, and 19 Under 35 U.S.C. § 103 is proper?

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claim 3. Accordingly, we reverse.

With respect to independent claim 3, it is analogous to claim 5 except that the interruptible instruction is at the front of the instruction block (claim 3, line 5). The Examiner's rejection is on the same basis as that of claim 3, with the Blandy reference added to show that front placement of interruptible instructions is known. Appellants' arguments and the Examiner's rejection correspond to those of claim 5 above. The Examiner's rejection of claim 3 shares the same deficiency noted above with respect to the rejection of claim 5. No motivation has been provided for placing the interruptible instruction at either the front or end of the instruction block. Therefore, Appellants' arguments are persuasive and we will not sustain the Examiner's rejection under 35 U.S.C. § 103.

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Conclusion

In view of the foregoing discussion, we have reversed the rejection under 35 U.S.C. § 103 of claims 3, 5, 6, 9, 12, 14, 15, and 18-20.

REVERSED

JERRY SMITH)	
Administrative Patent Judge)	
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)	
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)	BOARD OF PATENT
MICHAEL R. FLEMING)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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