

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SUSAN ELIZABETH EISEN AND
JAMES EDWARD PHILLIPS

Appeal No. 2003-1110
Application No. 09/295,439

ON BRIEF

Before OWENS, GROSS and BARRY, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal is from the final rejection of claims 27-48, which are all of the claims pending in the application.

THE INVENTION

The appellants claim a data processing system and method having out-of-order instruction execution. Claims 27 and 38 are illustrative:

27. A data processing system, comprising:

a first execution unit;

a second execution unit;

an input circuit for receiving a first plurality of instructions;

detection means for asserting a first dependency indicated in response to detecting a dependency between a first one of the first plurality of instructions, and a second instruction, wherein the dependency occurs during an interval when the second instruction is executed by the first execution unit; and

issue means, capable of issuing the first one of the plurality of instructions to either of the first and second execution units, for selectively issuing the first one of the plurality of instructions to one of the execution units in response to an indication by the first dependency indicator indicating that the dependency is being cleared.

38. A method, in a data processing system having a first execution unit and a second execution unit, comprising the steps of:

receiving a first plurality of instructions;

detecting a dependency between a first one of the first plurality of instructions and a second in-

Appeal No. 2003-1110
Application No. 09/295,439

issuer unit (498) with a bit map of the instructions that are suitably unconstrained to be executed (col. 33, lines 20-23 and 28-31). Instructions that carry dependencies are logically removed from the bitmap (col. 33, lines 31-33). The instruction issuer unit provides control signals for initiating and subsequently managing the execution of instructions to the register rename unit and selectively to parallel functional units (478_{0-n}) (col. 32, lines 33-34; col. 33, lines 38-42). A bypass control unit (520) monitors the status of the functional units and, in conjunction with the register references provided from the register rename unit, determines whether data is to be routed from a register file (472) to the functional units, or whether data being produced by the functional units can be immediately routed via a bypass unit (474) to a functional unit distribution bus (480) for use in executing a newly issued instruction scheduled by the instruction issuer unit (col. 33, lines 52-61).

The examiner's explanation of the rejection of claims 27 and 38 is as follows (answer, pages 4-5):

3. Nguyen et al. taught the invention (claims 27-28) including a data processing system comprising a first execution unit and a second execution (478₀ - 478_n); detection means (494, col. 48, lines 34-60); issue means and clearing means (col. 33, lines 28-65; col. 51, lines 1-20; fig. 14).

* * *

8. Claims 38-48 fail to teach or define above or beyond claims 27-37 and are rejected for the reasons set forth, supra.

"Anticipation requires that every limitation of the claim in issue be disclosed, either expressly or under principles of inherency, in a single prior art reference." *Corning Glass Works v. Sumitomo Electric*, 868 F.2d 1251, 1255-56, 9 USPQ2d 1962, 1965 (Fed. Cir. 1989). The appellants' claim 27 requires an issue means for selectively issuing a first one of a first plurality of instructions to one of two execution units in response to an indication by a first dependency indicator indicating that a dependency between that instruction and a second instruction is being cleared. Claim 38 requires selectively issuing a first one of a first plurality of instructions to one of two execution units in response to a detected dependency between that instruction and a second instruction being cleared prior to an availability of a result from the second instruction. The examiner, in the explanation of the rejection of claims 27 and 38

Appeal No. 2003-1110
Application No. 09/295,439

does not point out where these claim requirements are disclosed, either expressly or inherently, in Nguyen.

In the response to the appellants' arguments, the examiner argues (answer, pages 11-12):

It should be noted that the [Nguyen] instruction[s] that have a register dependency are logically removed. One of ordinary skill in the art would be aware that this would require a signal or indicator to inform the system that a dependency exist[s], further one of ordinary skill in the art would be aware that, the clearing an indicator would be to indicate to the system that the dependency no longer exist[s] and that such information would be sent to the instruction issuer, this is clearly taught in the cited passages.

This argument is not persuasive even if it is correct. The reason is that what the appellants' claims require is not an indication that a dependency no longer exists. Claim 27 requires issuing a first instruction to one of two execution units in response to an indication that a dependency is being (not has been) cleared. Claim 38 requires issuing a first instruction to one of two execution units in response to a detected dependency

Appeal No. 2003-1110
Application No. 09/295,439

being cleared prior to (not after) an availability of a result from a second instruction.

We therefore find that the examiner has not carried the burden of establishing a *prima facie* case of anticipation of the appellants' claimed invention.

DECISION

The rejection of claims 27-48 under 35 U.S.C. § 102(e) over Nguyen is reversed.

REVERSED

TERRY J. OWENS)
Administrative Patent Judge)
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) BOARD OF PATENT
ANITA PELLMAN GROSS) APPEALS AND
Administrative Patent Judge) INTERFERENCES
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LANCE LEONARD BARRY)
Administrative Patent Judge)

TJO/dpv

Appeal No. 2003-1110
Application No. 09/295,439

KELLY K. KORDZIK
WINSTEAD, SECHREST & MINICK, PC
1201 ELM STREET
DALLAS, TX 75270-2199