

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 38

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ERIC N. MANN

Appeal No. 2003-1281
Application 08/991,232

ON BRIEF

Before HAIRSTON, BARRY, and MACDONALD, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 21. In an Amendment After Final (paper number 30), claim 1 was amended.

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The disclosed invention relates to a programmable logic circuit, a microcontroller and a memory array located on a single integrated circuit chip.

Claims 1 and 9 are illustrative of the claimed invention, and they read as follows:

1. A circuit comprising:

a programmable logic circuit;

a microcontroller connected to said programmable logic circuit through a first bus;
and

a memory array connected to said microcontroller through a second bus, wherein said microcontroller, said programmable circuit, said memory array, said first bus and said second bus are fabricated as a single integrated circuit chip.

9. A circuit comprising:

a programmable logic circuit;

means for processing information connected to said programmable logic circuit through a first bus; and

a memory array connected to said processing means through a second bus, wherein said programmable logic circuit, said memory array, said first bus, said second bus, and said processing means are fabricated on a single integrated circuit chip.

The references relied on by the examiner are:

Narasimhan et al. (Narasimhan)	5,287,017	Feb. 15, 1994
Zavracky et al. (Zavracky)	5,656,548	Aug. 12, 1997

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Claims 1, 9 and 21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Zavracky.

Claims 2 through 8 and 10 through 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zavracky in view of Narasimhan.

Reference is made to the briefs (paper numbers 33 and 35) and the answer (paper number 34) for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will sustain the anticipation rejection of claim 9, reverse the anticipation rejection of claims 1 and 21 and reverse the obviousness rejection of claims 2 through 8 and 10 through 20.

Turning first to the anticipation rejection of claims 1, 9 and 21, Zavracky discloses a programmable logic circuit 802, a microcontroller 804 and 806, and a memory array 808 stacked on a single integrated circuit chip 800 (Figure 13; column 12, lines 29 through 39).

Appellant argues throughout the briefs that the circuit structure in Zavracky is neither "fabricated as a single integrated circuit chip" (claims 1 and 21) nor "fabricated on a

single integrated circuit chip" (claim 9).

The examiner contends (answer, page 8) that:

It's understood that a single integrated circuit chip as presently claimed, a circuit having a microcontroller, a programmable circuit, a memory array, a first bus and second bus are fabricated as a single integrated circuit chip just as Zavracky's processor chip having microprocessor, programmable logic array, [and] memory array. Each of the units communicate with each other by its own buses in the vertical direction and all of them are stacked together and fabricated as a multiple-layers processor chip. A processor chip having [a] plurality of layers still is a single chip or a single integrated circuit chip as claimed "a single integrated circuit chip" as Appellant argues"

By the examiner's own admission, the circuit structure in Zavracky (Figure 13) is "stacked together and fabricated as a multiple-layers processor chip." Such a multi-layered structure is not fabricated as a "single integrated circuit" chip as required by claims 1 and 21 because the microprocessor 804 and 806 and the memory array 808 are stacked as separate layers on the already fabricated "single integrated circuit chip." Stated differently, the programmable logic circuit 802 is the only circuit structure "fabricated as a single integrated circuit chip." Thus, the anticipation rejection of claims 1 and 21 is reversed because Zavracky does not disclose all of the limitations of these claims. Glaxo Inc. v. Novopharm Ltd., 52

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F.3d 1043, 1047, 34 USPQ2d 1565, 1567 (Fed. Cir. 1995).

Claim 9 differs from claims 1 and 21 because it merely requires that all of the circuit structure be "fabricated on a single integrated circuit chip." When claim 9 is given its broadest reasonable interpretation, we find that the vertical circuit structure disclosed by Zavracky (Figure 13) is indeed "fabricated on a single integrated circuit chip." During examination proceedings, a claim is given its broadest reasonable interpretation consistent with the specification. In re Morris, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1028 (Fed. Cir. 1997). Nothing in the disclosed and claimed invention precludes fabrication in a vertical direction on the single integrated circuit chip disclosed by Zavracky. Accordingly, the anticipation rejection of claim 9 is sustained.

Turning to the obviousness rejection of claims 2 through 8 and 10 through 20, we find that the examiner's reasoning (answer, pages 5 and 6) for combining the two references is not based upon the evidence of record. An obviousness rejection can not be based upon unsupported conclusory statements made by the examiner. In re Lee, 277 F.3d 1338, 1345, 61 USPQ2d 1430, 1435 (Fed. Cir. 2002). Even if we assume for the sake of argument that it would have been obvious to one of ordinary skill in the

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art to combine the teachings of the references, we additionally find that Narasimhan does not cure the noted shortcoming in the teachings of Zavracky (claims 2 through 8 and 11 through 20), and does not disclose a programmable logic circuit "selected from the group consisting of: a complex programmable logic device (CPLD) and a programmable logic array (PLA)" (claim 10). In summary, the obviousness rejection of claims 2 through 8 and 10 through 20 is reversed.

DECISION

The decision of the examiner rejecting claims 1, 9 and 21 under 35 U.S.C. § 102(e) is affirmed as to claim 9, and is reversed as to claims 1 and 21. The decision of the examiner rejecting claims 2 through 8 and 10 through 20 under 35 U.S.C. § 103(a) is reversed. Accordingly, the decision of the examiner is affirmed-in-part.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LANCE LEONARD BARRY)	APPEALS AND
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ALLEN R. MACDONALD)	
Administrative Patent Judge)	

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CHRISTOPHER P. MAIORANA, P.C.
24840 HARPER
ST. CLAIR SHORES MI 48080