

The opinion in support of the decision being entered today was **not** written for publication and is **not** precedent of the Board.

Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FERNANDO GONZALEZ, MIKE VIOLETTE,
NANSENG JENG, AFTAB AHMAD
and KLAUS SCHUEGRAF

Appeal No. 2003-1298
Application No. 09/369,579

ON BRIEF

Before KIMLIN, GARRIS and PAWLIKOWSKI, **Administrative
Patent Judges**.

PAWLIKOWSKI, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C.
§ 134 from the examiner's final rejection of claims
1-5, 21, 23-29, 33, 34, and 38-40.

Claims 1 and 34 are representative of the
subject matter on appeal, and are set forth below:

1. An isolation structure, comprising:
a semiconductor substrate having first and second separate active regions each extending to a top surface of the semiconductor substrate;
a field oxide region having a convex top surface opposite a convex bottom surface, wherein:
the convex bottom surface extends within said semiconductor substrate below said top surface of said semiconductor substrate, and
the convex top surface extends above the top surface of the semiconductor substrate;
a first isolation trench filled with an oxide dielectric material, extending into the semiconductor substrate, and extending above the top surface of the semiconductor substrate, wherein:
the first isolation trench has first and second opposite sides;
the first side of the first isolation trench makes contact with the field oxide region;
the second side of the first isolation trench makes contact with the first active region; and
said material filling said first isolation trench constitutes a structural barrier between the opposite sides of said first isolation trench that separates said field oxide region from said first active region, thus preventing the contact between said first active region and said field oxide region and preventing the encroachment of material from said field oxide region into said first active region;
a second isolation trench filled with said oxide dielectric material, extending into the semiconductor substrate, and extending above the top surface of the semiconductor substrate, wherein:
the second isolation trench has first and second opposite sides;
the first side of the second isolation trench makes contact with the field oxide region;
the second side of the second isolation trench makes contact with the second active region; and
said material filling said second isolation trench constitutes a structural

barrier between the opposite sides of said second isolation trench that separates said field oxide region from said second active region, thus preventing the contact between said second active region and said field oxide region and preventing the encroachment of material from said field oxide region into said second active region.

34. An isolation structure including a semiconductor substrate having a top surface, the isolation structure comprising:

a pair of dielectric structures each of which contacts a respective active region in the semiconductor substrate, comprises oxide, and rises lower above the top surface of the semiconductor substrate than a substantially oval field oxide region extending into the semiconductor substrate, wherein the field oxide region has opposite sides each of which makes contact with the deposited oxide of a respective one of the dielectric structures, wherein each one of said pair of dielectric structures constitutes a structural barrier that separates said respective active region from said field oxide region, thus preventing the encroachment of material from said field oxide region into said respective active region; and

nitride layers upon respective oxide layers, each said oxide layer contacting one of said dielectric structures and one of the active regions, and wherein each one of said pair of dielectric structures constitutes a structural barrier that separates said substantially oval field oxide region from each of said nitride layers.

Claims 1, 4, and 5 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kawamura.

Claims 21, and 23-25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kawamura.

Claims 26 and 29 stand rejected under 35 U.S.C. § 102(b) as being anticipated Kawamura.

Claim 33 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Kawamura.

Claims 38-40 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kawamura.

Claims 2, 3, 27, and 28 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kawamura as applied to claims 1 and 26 and further in view of Park.

Claim 34 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Vasquez.

The examiner relies upon the following references as evidence of unpatentability:

Vasquez	5,455,194	Oct. 3, 1995
Park	5,360,753	Nov. 1, 1994
Kawamura	5,096,848	March 17, 1992

Appellants group the claims as follows: Group I: claims 1-5; Group II: claims 21, and 23-24; group III claims 26-29; Group IV: claim 33; Group V: claim 34; and Group VI: claims 38-40. Brief, page 4. Insofar as the claims have been separately argued, we will address the claims separately. See 37 CFR § 1.192(c) (7) and (8) (2002).

OPINION

For the reasons set forth below, we reverse the rejection of claim 34 under 35 U.S.C. § 102(b) as being anticipated by Vasquez, but affirm all other rejections.

We note that in appellants' brief, with regard to all of the 35 U.S.C. § 102(b) rejections involving Kawamura (which address claims 1, 4, 5, 21, 23-25, 26, 29, 33, and 38-40), appellants provide the same arguments. Appellants argue that Kawamura does not anticipate the claims with regard to items (a), (b), and (c), summarized on pages 4-5 of the brief. Hence, our consideration of these items will address each of the 35 U.S.C. § 102(b) rejections over Kawamura, which in turn will address claims 1, 4, 5, 21, 23-25, 26, 29, 33, and 38-40.

Beginning with item (a), appellants argue that Kawamura does not anticipate the claimed subject matter regarding first and second separate active regions each extending to a top surface of the semiconductor substrate. Appellants argue that Kawamura does not set forth a teaching "of where such an active region is located in silicone substrate one." In rebuttal, the examiner, on pages 14-15 of the answer, sets forth a reasonable explanation that in fact active regions exist in the areas covered by resist pattern 4, and the examiner explains that the Figures 1A-K of Kawamura shows a resist pattern 4 that covers area on both sides of field oxide 9. Because appellants do not explain how an active layer could not exist in the area covered by resist pattern 4, we agree with the examiner's position.

With regard to item (b), appellants argue that the field oxide region has a convex top surface opposite a convex bottom

surface and that Kawamura's oxide region does not have a convex shape. Brief, page 5. In response, the examiner first points out that appellants' drawings are not drawn to scale. We agree. Most importantly, however, the examiner points out that the field oxide of Kawamura is formed in the same manner in which appellants' field oxide is formed. Due to the fact that the same process is utilized, we agree with the examiner that a similar shapes would result, absent evidence to the contrary. It is well settled that the Patent Office can require appellants to prove that a function or property relied upon for novelty is not possessed by prior art compounds otherwise meeting the limitations of the claims. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977). Here, appellants have not provided such proof. We therefore agree with the examiner's position on this issue.

With regard the item (c), appellants argue that the claimed subject matter requires first and second isolation trenches, each with second sides that respectively make contact with first and second active regions. Appellants argue that Kawamura does not provide such a teaching. In response, on page 16 of the answer, the examiner explains that trenches 11 of Kawamura contact the regions that were covered by resist pattern 4 (the active regions). The examiner concludes that therefore Kawamura anticipates this aspect of the claim. We agree. Upon our review of Figure 1(j), we agree with the examiner that Figure 1(j) shows the a first side of trench 11 that contacts an active region, and a second side that contacts the silicon oxide film 9.

Accordingly, we affirm each of the 35 U.S.C. § 102(b) rejections as being anticipated by Kawamura which involve

claims 1, 4, 5, 21, 23, 24, 25, 26, 29, 33, and 38-40 as being anticipated by Kawamura.¹

II. The 35 U.S.C. § 103 rejection of claims 2, 3, 27 and 28 under 35 U.S.C. § 103 as being unpatentable over Kawamura, as applied to claims 1 and 26, and further in view of Park

On page 11 of the brief, appellants argue that, for the same reasons (discussed above), Kawamura does not teach or suggest a number of features recited in claims 1 and 26. Appellants argue that Park provides no teaching to remedy the deficiencies of Kawamura.

However, as determined above, we do not agree with appellants that Kawamura is deficient, and we therefore determine that the examiner's rejection of these claims, as presented on pages 13-14 of the answer, sets forth a prima facie case obviousness.

We therefore affirm this rejection.

III. The 35 U.S.C. § 102(b) rejection of claim 34 as being anticipated by Vasquez

In this rejection, appellants argue that Vasquez does not disclose a pair of dielectric structures, each of which contacts a respective active region in a semiconductor substrate, and each one of the pair of dielectric structures constitutes a structural barrier that separates

¹Again, we note that for each grouping of claims (claims 1-5, claims 21 and 23-25, claims 26-29, claim 33 and claims 38-40), appellants presented the same arguments. Accordingly, we are able to determine the issues for each of these claims based on the analysis presented above.

a substantially oval field oxide region from each of the nitride layers. Brief, pages 8-9.

Appellants' Figure 6 depicts nitride layer 16 and trenches 34. Trenches 34 constitute a structure barrier that separates the substantially oval field oxide region 42 from each of the nitride layer 16. Dielectric structures 34 each contact a respective active region 44.

The examiner refers to Figure 5b of Vasquez and states that Vasquez discloses a pair of dielectric structures 24, each of which contacts a respective active region in the semiconductor substrate 10, and each pair of dielectric structures 24 constitutes a structural barrier that separates the respective active region from the field oxide region 44. Also, the examiner states that nitride layers 20 upon respective oxide layers 18 is disclosed and each oxide layer 18 contacts one of the dielectric structures 24 and one of the active regions in the semiconductor substrate 10 and each pair of dielectric structures 24 constitutes a structured barrier that separates the substantially oval field region 44 from each of the nitride layers 20.

On pages 9-10 of the brief, appellants argue that Vasquez does not teach this aspect of the claimed invention because Figure 5b of Vasquez shows that isolation region 44 contacts the edges of nitride layers 20 above the pair of trenches 24.

In rebuttal, on pages 17-18 of answer, the examiner states that in reviewing appellants' Figure 6, structure 34 is oxide, structure 22 (42) is oxide, and oxide 34 contacts nitride mask 16. As a device, the examiner states there is no separation between oxide structure 22 (42)/34, because

the material of the field oxide 22 (42) and that of the trench 34 are each oxide, and therefore they make-up one oxide structure. In this manner, the examiner asserts that the word "separates" as claimed is incorrect.

Claim 34 is reproduced again, below, with text in bold for emphasis:

34. An isolation structure including a semiconductor substrate having a top surface, the isolation structure comprising:

a pair of dielectric structures each of which contacts a respective active region in the semiconductor substrate, comprises oxide, and rises lower above the top surface of the semiconductor substrate than a substantially oval field oxide region extending into the semiconductor substrate, wherein the field oxide region has opposite sides each of which makes contact with the deposited oxide of a respective one of the dielectric structures, **wherein each one of said pair of dielectric structures constitutes a structural barrier that separates said respective active region from said field oxide region, thus preventing the encroachment of material from said field oxide region into said respective active region;** and

nitride layers upon respective oxide layers, each said oxide layer contacting one of said dielectric structures and one of the active regions, and **wherein each one of said pair of dielectric structures constitutes a structural barrier that separates said substantially oval field oxide region from each of said nitride layers.**

Referring to appellants' Figure 6, we find that claim 34 requires that the dielectric structures 34 are between the field oxide region 42 and nitride layers 16 and between the field oxide region 42 and active regions 44. In this way, the word "separates" is used. Comparing this subject matter with Figure 5B of Vasquez, we provide the following.

Figure 5B of Vasquez shows dielectric structures 24 between field oxide region 44 and nitride layer 20 and between field oxide region 44 and active regions of substrate 10.

Appellants do not explain why there could not be active regions located in substrate 10, below layer 20. We therefore agree with the examiner that dielectric structures 24 are between field oxide region 44 and active regions of substrate 10.

However, with respect to whether dielectric structures 24 are between oxide 44 and nitride layer 20, we find that Vasquez teaches that portions of layer 30 (shown in Figure 3) are removed, as shown in Figure 4. Then layer 42 is deposited thereon, as shown in Figure 4. Layer 42 is oxidized to form isolation region 44, shown in Figure 5A. See also column 5, lines 48-66 of Vasquez. Hence, no part of layer 30 (which forms vertical wall surfaces 24) is between oxide 44 and nitride layer 20. Hence, we agree with appellants that because plug 34 is already formed prior to formation of isolation region 44, dielectric structures 24 do not separate nitride layer 20 from oxide region 44.

In view of the above, we reverse the rejection of claim 34.

IV. Conclusion

We reverse the rejection of claim 34, but affirm every other rejection.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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