The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID DONGGANG WU

Appeal No. 2003-1315
Application No. 09/503,838

ON BRIEF

Before HAIRSTON, BARRETT, and BARRY, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 14, 16 and 17.

The disclosed invention relates to a method for testing a semiconductor chip by determining the parasitic capacitance of a dummy structure in the semiconductor chip, storing the parasitic capacitance value in memory, and then analyzing a test structure

in the semiconductor chip using the stored parasitic capacitance value.

Claim 1 is the only independent claim on appeal, and it reads as follows:

1. A method for testing a semiconductor chip, the method comprising:

providing a test structure and a dummy structure in the semiconductor chip, wherein the dummy structure has a structure that replicates the test structure except having a discontinuity that disables the dummy structure;

coupling to the dummy structure and determining the parasitic capacitance of the dummy structure; and

coupling to the test structure and analyzing the test structure using the determined parasitic capacitance of the dummy structure; and

storing the determined parasitic capacitance of the dummy structure in a memory device, and wherein analyzing the test structure using the determined parasitic capacitance of the dummy structure includes accessing the stored parasitic capacitance.

The references relied on by the examiner are:

Aeba	5,466,956	Nov. 14, 1995
Akram et al. (Akram)	6,022,750	Feb. 8, 2000

"Multi-Chip Probe Card for Capacitance Voltage Measurements," IBM Technical Disclosure Bulletin, Vol. 25, pp. 5736-37 (Apr. 1, 1983)(Hereinafter referred to as IBM TDB).

Olowolafe, "*C-V* Profiles," Wiley Encyclopedia of Electrical and Electronics Engineering Online, (Univ. of Del., Dec. 27, 1999).

Claims 1 through 4, 13, 14 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Aeba in view of Olowolafe.

Claims 5 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Aeba in view of Olowolafe and admitted prior art.

Claims 7 through 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Aeba in view of Olowolafe and the IBM TDB.

Claims 11, 12 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Aeba in view of Olowolafe and Akram.

Reference is made to the briefs (paper numbers 13 and 15) and the answer (paper number 14) for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the 35 U.S.C. § 103(a) rejection of claims 1 through 14, 16 and 17.

The examiner states (answer, page 4) that “Aeba (US 5,466,956) discloses a method of making and testing a

semiconductor device which comprises the following steps: providing a test structure **A2** and a dummy structure **A1** on a semiconductor chip **9** where the dummy structure replicates the test structure except for a discontinuity that disables the dummy structure [column 4, lines 55-65], coupling to the dummy structure and determining the parasitic capacitance C_y [column 5, lines 25-30], coupling to the test structure and analyzing the test structure using the known parasitic capacitance [column 5, lines 30-37]." The examiner acknowledges (answer, page 4) that "Aeba does not disclose the storing and accessing the stored parasitic capacitance in a memory device." Since Olowolafe "teaches the use of a computer when making C-V measurements [Figure 9]," the examiner concludes (answer, page 4) that "[i]t would have been obvious to one of ordinary skill in the art to store and access the store[d] parasitic capacitance in the method of Aeba since computers are commonly used in C-V measurement systems and since Aeba is directed towards analyzing the test structure."

Appellant argues (brief, page 6) that areas A1 and A2 are not test and dummy structures, respectively, and that Aeba neither teaches nor would have suggested to one of ordinary skill

in the art a “dummy structure having a structure that replicates the test structure.” Appellant additionally argues (brief, page 7) that the applied references neither teach nor would have suggested the claimed step of accessing and using the stored parasitic capacitance when analyzing the test structure.

Aeba explains (column 3, lines 24 and 25; column 5, lines 26 through 30) that both the electrode 7 on first bonding pad area A1 and bonding pad 6a on second bonding pad area A2 are contacted by probes of a capacitance measurement system to determine the capacitance of the interlayer insulator film 4 that interrupts the conductor path between the bonding pad 6a, wiring conductor 3a and electrode 7. In other words, Aeba is measuring the capacitance of the insulator film 4 which serves as a “discontinuity” in “a dummy structure.” If the discontinuity makes the structure a dummy structure, then Aeba does not disclose a test structure. Thus, we agree with the appellant’s argument that the dummy structure in Aeba does not replicate a test structure as required by the claims on appeal.

We agree with the examiner that Olowolafe uses a computer when making C-V measurements, but we disagree with the examiner’s conclusion that the skilled artisan would have known to access a

stored parasitic capacitance value of a dummy structure when analyzing a test structure. But for appellant's disclosed and claimed invention, nothing in the record before us teaches or would have suggested such a step to the skilled artisan.

In view of the foregoing, the obviousness rejection of claims 1 through 4, 13, 14 and 16 is reversed.

The obviousness rejections of claims 5 through 12 and 17 are reversed because the admitted prior art, the IBM TDB and Akram fail to cure the noted shortcomings in the teachings of Aeba and Olowolafe.

DECISION

The decision of the examiner rejecting claims 1 through 14, 16 and 17 under 35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)
LEE E. BARRETT Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)

KWH:hh

CRAWFORD, PLLC
1270 NORTHLAND DR.
STE. 390
ST. PAUL, MN 55120