

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 30

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DENNIS J. HERRELL
and THOMAS P. DOLBEAR

Appeal No. 2003-1361
Application 09/099,758

ON BRIEF

Before HAIRSTON, JERRY SMITH, and NAPPI, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 16 and 52 through 54.

The disclosed invention relates to an apparatus comprising an integrated circuit carrier, a circuit board and a loop circuit having a loop inductance that is defined from a first group of

circuit board vias and a first group of carrier vias to a first side of the circuit carrier, and then through a second group of carrier vias and a second group of circuit board vias.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. An apparatus comprising:

an integrated circuit carrier including:

first and second groups of carrier vias extending substantially from a first side of said carrier towards a second side of said carrier;

a circuit board including:

first and second groups of circuit board vias extending substantially from a first side of said circuit board towards a second side of said circuit board;

a loop circuit having a loop inductance, said loop circuit defined from said first group of circuit board vias, through said first group of carrier vias to said first side of said circuit board and back through said second group of carrier vias, through said second group of circuit board vias;

wherein said carrier vias of said first and second groups are arranged in an anti-parallel tessellation and include a substantial majority of all carrier vias for coupling respective power supply voltages; and

wherein said circuit board vias of said first and second groups are arranged in an anti-parallel tessellation and include a substantial majority of all circuit board vias for coupling respective power supply voltages.

The references relied on by the examiner are:

Hernandez	4,754,366	June 28, 1988
Sudo et al. (Sudo)	5,475,264	Dec. 12, 1995
Patil et al. (Patil)	5,672,911	Sept. 30, 1997
Forehand et al. (Forehand)	5,847,936	Dec. 8, 1998
		(filed June 30, 1997)

Claims 1, 6 through 13, 16 and 52 through 54 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sudo in view of Forehand.

Claims 2 through 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sudo in view of Forehand and Patil.

Claims 14 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sudo in view of Forehand and Hernandez.

Reference is made to the brief (paper number 27) and the answer (paper number 28) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejections of claims 1 through 16 and 52 through 54.

The examiner has made findings (answer, page 1) that:

[F]irst and second groups of carrier vias 54-1 and 54-2 [in Sudo] have an arrangement of multiple, parallel oriented conductive structures of the loop circuit, and wherein current flows through a first group of the conductive structures is in an opposing direction to the current flow through a second group of the conductive structures. It is noted that the loop circuit as disclosed in Fig. 12 of Sudo et al would be considered as a loop circuit having a loop inductance because the mutual loop inductance would be formed when the current flow through the first and second groups of complementary power carrier vias.

According to the examiner (answer, page 2):

Sudo et al do further disclose that the loop circuit of the closest power vertical conductive paths 15 and 16 arranged in Fig. 11 or the loop circuit arranged in

Fig. 12 causes the decreasing of "unwanted inductance present in the multilevel thin film wiring layers 22" (column 5, lines 5-11). Accordingly, one skilled in the art would [have] recognized that the loop circuit arranged in Fig. 12 of Sudo et al would have properties of reduction in the inductance because it has been held that when the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent.

Appellants argue (brief, pages 8 and 12) that the power supply vias taught by Sudo (Figures 11 and 12) are not in a loop circuit as claimed, and that such a loop circuit is neither expressly nor inherently disclosed in the applied references.

We agree with appellants' arguments. We find that Sudo does not disclose a loop circuit because the Figure 11 embodiment does not show a connection between the ground pad electrode 16 and the already connected LSI chip 23 and power supply pad electrode 15. Thus, the appellants correctly argue (brief, pages 14 and 15) that:

First, as a preliminary matter, no circuit involving vias 15 and 16 is disclosed. Second, no reasonable interpretation of FIG. 11 supports the conclusion that such a circuit is necessarily inherent. In fact, the reasonable interpretation of FIG. 11 is that any complementary, opposing direction current that would flow through a return circuit path . . . involves a via well removed from via 15 However, whatever the actual location, no reasonable interpretation of FIG. 11 supports the argument that via 16 is necessarily the return path. Accordingly, *Sudo* simply does not disclose a loop circuit, as claimed.

In view of the foregoing, the obviousness rejection of

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claims 1, 6 through 13, 16 and 52 through 54 is reversed because we additionally agree with the appellants' argument (brief, page 15) that the teachings of Forehand, whether considered alone or in combination with Sudo, would not have rendered obvious the claimed invention.

The obviousness rejections of claims 2 through 5, 14 and 15 are reversed because the teachings of Patil and Hernandez fail to cure the noted shortcoming in the teachings of Sudo and Forehand.

DECISION

The decision of the examiner rejecting claims 1 through 16 and 52 through 54 under 35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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JERRY SMITH)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
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