

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TUAN D. PHAM, MARK T. RAMSBY, SAMEER S. HADDAD,
ANGELA T. HUI, YU SUN, CHI CHANG

Appeal No. 2003-1365
Application No. 09/376,659¹

ON BRIEF²

Before HAIRSTON, DIXON and SAADAT, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1-7, 10-17, 21 and 22. Claims 8, 9 and 18-20 have been canceled.

We affirm.

BACKGROUND

¹ Application for patent filed August 18, 1999.

² A request for oral hearing was waived in a communication filed August 19, 2003.

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Appellants' invention is directed to a method of fabricating semiconductor memory devices while reducing mobile ion migration into transistor gate sides during semiconductor manufacturing. After the gate stacks, which includes a control gate and a floating gate, the subsequent processing steps cause mobile ions and/or other process-induced charges migrate into the sides of the floating gate and alter the electrical characteristics of the device (specification, page 2). According to Appellants, the gate stacks are covered with a first protective layer which is partially etched away to expose the intended source regions and to allow dopants be implanted into the source regions (specification, page 2). A second protective layer is then deposited onto the first layer and partially etched away to expose the intended drain regions and allow dopants be implanted into the drain regions (id.). Subsequent manufacturing steps may be carried out while the first and the second protective layers protect the sides of the gate stacks from ion migration into the floating gate area (id.).

Representative independent claims 1 and 10 are reproduced
bellow:

1. A method for establishing plural core gate transistors
on a semiconductor substrate, comprising:

forming plural core gate stacks on the substrate, each core
gate stack having at least one side;

covering the core gate stacks with a first protective layer;

etching away portions of the first layer such that at least
intended source regions of the substrate are exposed;

implanting dopant into the intended source regions;

depositing a second protective layer onto the first layer,
the second protective layer including high temperature oxide
(HTO);

etching the second protective layer such that at least
intended drain portions of the substrate are exposed;

implanting dopant into the intended drain regions to thereby
establish plural core transistors; and

undertaking subsequent manufacturing acts with first and
second layers protecting at least the sides of the core gate
stacks.

10. A method for making a flash memory device, comprising:

forming first and second protective shoulders on core gate
stacks, such that dopant can be implanted into a substrate
supporting the stacks to establish transistors and such that
charge migration into sides of the gate stacks during interlayer
dielectric(ILD) formation and device metallization is prevented,
at least the second shoulder including high temperature oxide
(HTO).

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The Examiner relies on the following references in rejecting the claims:

Gardner et al. (Gardner '518)	5,656,518	Aug. 12, 1997
Komori et al. (Komori)	5,656,522	Aug. 12, 1997
Gardner et al. (Gardner '531)	5,672,531	Sep. 30, 1997
Gardner et al. (Gardner '298)	5,789,298	Aug. 4, 1998
Kokubu	6,200,858	Mar. 13, 2001 (filed Aug. 3, 1999)
Pham et al. (Pham)	6,248,627	Jun. 19, 2001 (filed Aug. 18, 1999)

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner '298 in view of Kokubu.

Claims 1-5, and 10-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Komori in view of Gardner '298 and Kokubu.

Claims 6, 7, 16 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Komori in view of Gardner '298, Kokubu and Gardner '518.

Claims 21 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Komori in view of Gardner '298, Kokubu and Gardner '531.

Claims 1-7, 10-17, 21 and 22 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of U.S. Patent No. 6,248,627 (Pham) in view of Kokubu.

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We make reference to the answer (Paper No. 14, mailed September 25, 2002) for the Examiner's reasoning, and to the appeal brief (Paper No. 13, filed June 28, 2002) and the reply brief (Paper No. 16, filed November 25, 2002) for Appellants' arguments thereagainst.

OPINION

With respect to the 35 U.S.C. § 103 rejection of claim 10 over Gardner '298 and Kokubu, Appellants point out that Gardner '298 teaches a non-symmetrical spacer but does not address charge migration and the additional HTO sidewall spacer (brief, page 6). Appellants further refer to a first sidewall spacer mentioned at Column 5, line 43 of Gardner '298 as an additional element on the drain side of the gate stack and the use of a directional etch process differing from the recited features of claim 10 (id.). Additionally, Appellants argue that Gardner '298 mentions nothing about the problem of the gate bird's beak such that one of ordinary skill in the art would have been motivated to use the solution offered by Kokubu (brief, page 7 and reply brief, page 6). Appellants further assert that, without a basis for combining the references, the prevention of charge migration into the sides of the gate stacks cannot be inherent since inherency must be derived from one single reference and not from several

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improperly combined references (brief, page 8 and reply brief, pages 7 & 8).

The focus of the Examiner's arguments is that the teaching in support of the combination of the references need not be in the initial [primary] reference (answer, page 7). The Examiner also asserts that the reason to use the HTO film as a part of the sidewall structure of Gardner '298 is present in Kokubu whereas the prevention of charge migration into the sides of the gate stacks can be obtained from the implicit and/or inherent disclosure of the prior art reference (id.).

Before addressing the Examiner's rejection based upon prior art, it is an essential prerequisite that the claimed subject matter be fully understood and the scope of the claims be determined. Claim interpretation must begin with the language of the claim itself. See Smithkline Diagnostics, Inc. v. Helena Laboratories Corp., 859 F.2d 878, 882, 8 USPQ2d 1468, 1472 (Fed. Cir. 1988). Furthermore, the general claim interpretation principle that limitations found only in the specification of a patent or patent application should not be imported or read into a claim must be followed. See In re Priest, 582 F.2d 33, 37, 199 USPQ 11, 15 (CCPA 1978). "[T]he name of the game is the claim." In re Hiniker Co., 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529

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(Fed. Cir. 1998). Claims will be given their broadest reasonable interpretation consistent with the specification, and limitations appearing in the specification are not to be read into the claims. In re Etter, 756 F.2d 852, 858, 225 USPQ 1, 5 (Fed. Cir. 1985). Accordingly, we will initially direct our attention to Appellants' claim 10 and first determine its scope.

We note that while claim 10 recites that first and second protective shoulders be formed on core gate stacks, the claim does not require formation of the two layers on both sides of each gate stack before implantation, nor exposing the source or the drain portions of the substrate. The claim merely requires a two-layer protective shoulder on one or more side(s) of the gate stacks. In fact it is the presence of the protective shoulders that prevents charge migration into the sides of the gate stacks only where the shoulders are present. There is no other disclosed or claimed structure that contributes to blocking charge migration. Therefore, constructing claim 10 as broadly as possible, we note that if the protective shoulder layers are present, charge migration into the sides of the gate stacks are prevented.

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As a general proposition, in rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) and In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). A prima facie case of obviousness is established when the teachings of the prior art itself would appear to have suggested the claimed subject matter to one of ordinary skill in the art. See In re Bell, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993); In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992); Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985). In considering the question of the obviousness of the claimed invention in view of the prior art relied upon, the Examiner is expected to make the factual determination set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. See also In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998). However,

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the motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

After reviewing Gardner '298 we agree with the Examiner that the step of "forming first and second protective shoulders" is disclosed in the references as forming a first nitride protective shoulder 36 and a second protective shoulder 40 (answer, page 3). As depicted in Figure 7, the nitride spacer 36 and the oxide spacer 40 are formed on side 20 of a gate stack which block the dopants during ion implantation, and certainly, prevent charge migration during the subsequent process steps. We also observe that the thin oxide layer 30 (col. 5, lines 15-21) covering the gate stack and the entire substrate, which is apparently characterized by Appellants (brief, page 6) as an additional spacer, is the same oxide layer that is disclosed by Appellant (specification, page 4, lines 17-20) to cover the gate stacks. Therefore, this thin oxide layer is neither a part of the two-layer protective shoulders nor can be considered as an additional spacer.

A review of Kokubu, on the other hand, reveals that the reference relates to a semiconductor storage device having a floating gate and a specific structure for reducing the effect of thermal oxidation heat on uniformity of the insulating film under the floating gate (col. 1, lines 37-40). As depicted in Figure 8, Kokubu discloses a conventional memory structure having a side wall formed of thin thermal oxide 13-1 and thin layer of hot thermal oxide (HTO) 13-2 which is covered by CVD oxide film 13-3 (col. 1, lines 21-29). Although Kokubu reduces the time of the thermal oxidation of the gate oxide and prevents the formation of the bird's beak in the gate oxide area by using a specific arrangement of a first oxide film, a nitride film and a second oxide film on the side wall of a gate stack, as shown in Figures 1 and 5, it is readily apparent that the use of HTO as the second or a subsequent side wall layer over the first layer of either oxide or nitride is customary. The conventional memory device, as shown in figure 8 of Kokubu, nevertheless, includes a layer of HTO over a layer of oxide whereas the improvements offered by Kokubu prevents the formation of the gate bird's beak by using a gate stack protective layer of HTO/nitride/HTO (Figure 1) or of nitride/HTO/nitride/HTO (Figure 5).

Therefore, we find Appellants' arguments that because Gardner '298, as the primary reference, does not recognize the problem of the gate bird's beak, one of ordinary skill in the art would not have combined the references and have used HTO as the second side wall layer. In this case the reason for the modification comes not only from the benefits of preventing the gate bird's beak by using the particular HTO/nitride/HTO combination as the side wall layers in Kokubu, but from the fact that HTO is commonly used as the second layer in combination with a nitride or oxide layer and as a protective layer on the sides of gate stacks. Although one may accurately cite the prevention of the gate bird's beak as a reason for using the specific HTO/nitride/HTO configuration disclosed by Kokubu, the general teaching of the reference related to the use of HTO as the second side wall layer (described as the "Related Art" and depicted in Figure 8) leads one of ordinary skill in the art to successfully substitute HTO for oxide layer 38 of Gardner '298. In fact, the Examiner correctly recognizes the specific HTO and nitride layers combination disclosed by Kokubu as the remedy for the gate bird's beak but passes over the teachings related to the use of HTO as a conventional layer in side wall layers structure on the side of a gate stack. In view of the analysis above, we find the

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combination of Gardner '298 and Kokubu to be reasonable and sufficient to establish a prima facie case of obviousness. Accordingly, the 35 U.S.C. § 103 rejection of claim 10 over Gardner '298 and Kokubu is sustained.

Turning now to the 35 U.S.C. § 103 rejection of claims 1-5 and 10-15 over Komori, Gardner '298 and Kokubu, we note that the Examiner relies on Komori to characterize the first and second protective layers as layers 30 and 31 which are etched away to expose the source and the drain regions and on Kokubu and Gardner '298 for the first layer made of nitride and the second layer formed of HTO (answer, page 4). Appellants mainly dispute the manner in which the references are combined and the absence of any reason or suggestion for the combination (brief, pages 9-13 and reply brief, pages 9-11).

A review of Komori shows that the reference is concerned with customizing the impurity concentration and the junction depth of the source and drain regions in a field effect transistor that constitutes the non-volatile memory (col. 3, lines 28-34). Komori achieves the specific source and drain doping profile by introducing n-type and p-type impurities in a particular order and by limiting the doping to one of or both source and drain regions using photoresist masks. First,

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photoresist mask 30 is used to limit the introduction of n-type impurities 11n and 12n to the source region of p-well 3 (Figure 6 and col. 8 line 57-65) and then, photoresist mask 31 is used to limit the introduction of p-type impurities 13p to the drain region of p-well 3 (Figure 7 and col. 9, line 10-17). Komori further introduces n-type impurities 14n into both source and drain regions by applying and patterning photoresist mask 33 (Figure 8 and col. 9, lines 46-52). Therefore, what Komori uses for covering the gate stacks and exposing the source or the drain regions are photoresist masks which are completely etched away and removed after each implant. In other words, in contrast with the side wall layers of Gardner '298 and Kokubu, no parts of the masks in Komori remain on the structure to protect the sides of the gate stacks.

Although in our analysis of Gardner '298 and Kokubu above we concluded that the Examiner has properly combined the two references in rejecting claim 10, we agree with Appellants that there is no reason to add Komori to the combination. In that regard, while Komori uses photoresist masks for exposing the source and drain regions during the step of introducing impurities, the masks are entirely removed and no part of them are left on the sides of the gate stacks. Additionally, the

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Examiner has pointed to no teachings in the prior art, nor do we find any, that would have suggested to one of ordinary skill in the art to use the HTO and nitride side wall layers of Gardner '298 and Kokubu in the same manner the photoresist masks of Komori are used to limit the implanting of dopants to the exposed source and drain regions. As the Examiner has failed to establish a prima facie case obviousness, we cannot sustain the 35 U.S.C. § 103 rejection of claims 1-5 and 10-15 over Komori, Gardner '298 and Kokubu.

We note that the Examiner, in combination with Komori, Gardner '298 and Kokubu, further relies on Gardner '518 to reject claims 6, 7, 16 and 17 and on Gardner '531 to reject claims 21 and 22 under 35 U.S.C. § 103(a). Gardner '518 merely describes asymmetrical side walls (Figures 1H and 1I and Col. 5, lines 11-19) while Gardner '531 suggests SiON as a dielectric material to be used as the side wall (Col. 7, lines 63-67). By relying on these references, the Examiner has not provided any additional evidence to overcome the deficiencies of Komori, Gardner '298 and Kokubu as discussed above with respect to claims 1-5 and 10-15, and therefore, has failed to set forth a prima facie case of obviousness. Accordingly, we do not sustain the 35 U.S.C. § 103 rejection of claims 6, 7, 16 and 17 over Komori, Gardner '298 and

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Kokubu in view of Gardner '518 and of claims 21 and 22 over Komori, Gardner '298 and Kokubu in view of Gardner '531.

Turning now to the rejection of the claims under the judicially created doctrine of obviousness-type double patenting over Pham in view of Kokubu, we note that Appellants rely on the same arguments related to the lack of basis for combination that was raised with respect to the combination of Kokubu and Gardner '298 (brief, page 20 and reply brief, page 16). Additionally, Appellants rely on the common filing date of the instant application and the application that resulted in the patent to Pham and indicate that the rejection should not stand since there would be no extension of time (id.). In response, the Examiner reminds Appellants of common ownership as the other relevant aspect of the doctrine of obviousness-type double patenting and the possibility that the patent terms may not coincide (answer, page 10).

We agree with the Examiner and add that the claims of Pham are similar to the present claims under appeal to the extent that the patented independent claims 1 and 8 recite the same process steps and further require that the second protective layer be formed of nitride or SiON whereas the present claims require HTO as the second protective layer. As discussed above with respect

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to the rejection of claim 10, HTO is commonly used as the second layer in combination with a nitride or oxide layer as the side wall or protective layer on the sides of gate stacks. Therefore, one of ordinary skill in the art would have found the combination obvious and would have been led to successfully substitute HTO for the nitride or SiON layer of Pham.

As discussed above, the appealed claims recite the use of HTO, as suggested by Kokubu, for the second protective layer in the same process steps as those recited in claims of Pham. Accordingly, we sustain the rejection of claims 1-7, 10-17, 21 and 22 under the judicially created doctrine of obviousness-type double patenting over claims 1-14 of Pham (U.S. Patent No. 6,248,627) in view of Kokubu.

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CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1-7, 11-17, 21 and 22 under 35 U.S.C. § 103(a) is reversed, but is affirmed with respect to the rejection of claim 10 under 35 U.S.C. § 103(a) and of claims 1-7, 10-17, 21 and 22 under the judicially created doctrine of obviousness-type double patenting.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH L. DIXON)	APPEALS
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