

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board

Paper No. 30

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARK MCQUEEN

Appeal No. 2003-1367
Application 09/640,237

ON BRIEF

Before PAK, WARREN, and WALTZ, *Administrative Patent Judges*.

WARREN, *Administrative Patent Judge*.

This is an appeal under 35 U.S.C. § 134 from the decision of the examiner finally rejecting claims 1 through 11 and 14 through 18, which are all of the claims pending in this application.

Claims 1 and 8 are illustrative of the claims on appeal:

1. A method of forming a contact for a semiconductor device, comprising:
providing a semiconductor substrate having at least one active region;

depositing a first barrier layer over said substrate;
planarizing said first barrier layer;
forming a first opening through said first barrier layer to expose a portion of said active region;
filling said first opening with a first conductive material to form a contact plug;
forming an individual conductive contact land over said contact plug, said individual conductive contact land covering only a single contact plug;
depositing a second barrier layer over said first barrier layer and said individual conductive contact land;
forming a second opening through said second barrier layer to expose a portion of said individual conductive contact land; and
filling said second opening with a second conductive material to form said contact.

8. A method of producing a bipolar transistor for the dissipation of electrostatic discharges, comprising:

providing an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said drain region and said source region on said substrate active area;
depositing a first barrier layer substantially covering said at least one field oxide area, said at least one active area, and said at least one transistor gate member;
planarizing said first barrier layer to expose said at least one transistor gate member;
patterning a first etch mask on said first barrier layer, wherein said first etch mask includes openings substantially over said at least one drain region and over said at least one source region;
etching said first barrier layer to expose said at least one drain and said at least one source region in said substrate forming at least one drain via and at least one source via, respectively;
removing said first etch mask;
depositing a layer of first conductive material over said etched first barrier layer to fill said at least one drain via and said at least one source via;
planarizing said first conductive material forming at least one drain contact plug and at least one source contact plug in said at least one drain via and said at least one source via, respectively;

Appeal No. 2003-1367
Application No. 09/640,237

patterning a first deposition material on said first barrier layer and said at least one transistor gate member, wherein said first deposition material includes individual openings over each of said at least one drain contact plugs and each of said at least one source contact plugs;

depositing a layer of second conductive material over said first deposition material to fill said individual openings over each of said at least one drain contact plugs and each of said at least one source contact plugs;

planarizing said second conductive material to said first deposition material to form an individual drain contact land over each of said at least one drain contact plugs and an individual source contact land over each of said at least one source contact plug;

removing said first deposition material;

depositing a second barrier layer over said first barrier layer and said individual drain contact lands and said individual source contact lands;

patterning a second etch mask on said second barrier layer, wherein said second etch mask includes openings substantially over said individual drain contact lands and over said individual source contact lands;

etching said second barrier layer to expose said at least one drain contact land and said at least one source contact land forming at least one drain contact via and at least one source contact via, respectively;

removing said second etch mask;

depositing a layer of third conductive material over said etched second barrier layer to fill said at least one drain contact via and said at least one source contact via; and

planarizing said third conductive material forming at least one upper drain contact and at least one upper source contact in said at least one drain contact via and said at least one source contact via, respectively.

The appealed claim 1 is directed to a method of making a contact for a semiconductor device having a contact land covering only a single contact plug. The contact landing pads render the fabrication of semiconductor devices "less sensitive to alignment constraint in the formation of contacts." (Spec., page 6.) The appealed claim 8 is directed to a method of making a bipolar transistor for the dissipation of electrostatic discharges that includes the steps, among others, of forming an individual source contact land and "planarizing said first barrier layer to expose said at least one transistor gate member."

Appeal No. 2003-1367
Application No. 09/640,237

The references relied on by the examiner are:

| | | |
|----------------------------------|-----------|---------------|
| Hendrickson et al. (Hendrickson) | 4,735,914 | Apr. 5, 1998 |
| Nguyen et al. (Nguyen) | 5,914,518 | Jun. 22, 1999 |
| Maari | 5,925,917 | Jul. 20, 1999 |
| Nakamura et al (Nakamura) | 5,986,299 | Nov. 16, 1999 |
| Takebuchi | 6,018,195 | Jan. 25, 2000 |
| Clampitt | 6,081,033 | Jun. 27, 2000 |

The following grounds of rejection are advanced by the examiner on appeal:

claims 1, 2, 5, 7, and 18 stand rejected under 35 U.S.C. § 103(a) based on Nguyen and Nakamura;

claims 3 and 4 stand rejected under 35 U.S.C. § 103(a) based on Nguyen, Nakamura, and Maari;

claim 6 stands rejected under 35 U.S.C. § 103(a) based on Nguyen, Nakamura, and appellant's admitted prior art (Figs. 35-38, page 4, lines 26-29, and page 5, lines 1-5);

claims 8 and 9 are rejected are rejected under 35 U.S.C. § 103(a) based on Nakamura, Takebuchi, and appellant's admitted prior art (Figs. 35-38, page 4, lines 26-29, and page 5, lines 1-5);

claims 10 and 11 are rejected are rejected under 35 U.S.C. § 103(a) based on Nakamura, Takebuchi, appellant's admitted prior art (Figs. 35-38, page 4, lines 26-29, and page 5, lines 1-5), and Hendrickson;

claims 14 and 15 are rejected are rejected under 35 U.S.C. § 103(a) based on Nakamura, Takebuchi, appellant's admitted prior art (Figs. 35-38, page 4, lines 26-29, and page 5, lines 1-5), and Clampitt; and,

claims 16 and 17 are rejected are rejected under 35 U.S.C. § 103(a) based on Nakamura, Takebuchi, appellant's admitted prior art (Figs. 35-38, page 4, lines 26-29, and page 5, lines 1-5), and Maari.

Appellant groups the appealed claims into four separate groups (a) - (d). We note that group (d) encompasses claims 14 and 15, which are subject to only a single ground of rejection. Similarly, group (c) encompasses claims 8 and 9 which are subject to only a single ground of rejection. Groups (a) and (b), however, each encompass a group of claims in which all of the claims are not subject to a single ground of rejection.

Appeal No. 2003-1367
Application No. 09/640,237

37 CFR § 1.192(c)(7) (2002) provides in pertinent part:

For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to that ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable.

Accordingly, we decide this appeal based on claims 1, 3, 6, 8, 10, 14, and 16 as representative of the respective grounds of rejection because appellant has not submitted argument specifically addressing the patentability of one or more claims in any ground of rejection. 37 CFR § 1.192(c)(7)(2002); see *In re McDaniel*, 293 F.3d 1397, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002) ("*See* 37 CFR § 1.192(c)(7) (2001). If the brief fails to meet either requirement, the Board is free to select a single claim for each group of claims subject to a common ground of rejection as representative of all claims in that group and to decide the appeal of the rejection based solely on the selected representative claim.").

We affirm the grounds of rejection of claims 1 through 7 and 18. We reverse the grounds of rejection of claims 8 through 11 and 14 through 17 because we find that the examiner has failed to set forth a *prima facie* case of obviousness with respect to these claims. Accordingly, the decision of the examiner is affirmed-in-part.

Rather than reiterate the respective position advanced by the examiner and appellant, we refer to the examiner's answer and appellant's brief and reply brief for a complete exposition thereof.

Opinion

The first step in reviewing the application of the prior art to the appealed claims is to interpret the language of the claim by giving the claim terms their broadest reasonable interpretation consistent with the written description provided in appellant's specification as it would be interpreted by one of ordinary skill in the art. *See, e.g., In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000); *In re Morris*, 127 F.3d 1048, 1054-55,

Appeal No. 2003-1367
Application No. 09/640,237

44 USPQ2d 1023, 1027 (Fed. Cir. 1997); *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). The open-ended transitional phrase "comprising" opens claim 1 to encompass products which include at least the specified limitations of the claim as well as additional steps, elements, and materials. *In re Baxter*, 656 F.2d 679, 686-87, 210 USPQ 795, 802-03 (CCPA 1981) ("As long as one of the monomers in the reaction is propylene, any other monomer may be present, because the term 'comprises' permits the *inclusion* of other steps, elements, or materials").

We here consider the claim term "barrier layer" in the context of the claim as a whole, including consideration thereof in light of the specification, in which this term is used independently to refer to (1) a TEOS layer, (2) a BPSG, BSG, or PSG layer, and (3) a combination of a TEOS layer and a BPSG, BSG, or PSG layer. (Spec., page 6.) The specification additionally describes the layer **226** as an "insulative barrier layer." (Spec., page 4.) Thus, while the specification states that a TEOS layer prevents dopant migration, the specification also uses the term "barrier layer" broadly to refer to single layers of doped glass such as BPSG, BSG, and PSG, which are not taught to have the same dopant migration prevention properties as a TEOS layer. Accordingly, we find, consistent with its use in the specification, that the claim term "barrier layer" encompasses doped as well as undoped insulating layers, which need not prevent dopant migration to the same extent that a TEOS layer might. The claim term "planarizing said first barrier layer" requires application of a planarizing process to at least a portion of the first barrier layer. Finally, the term "contact land" is interpreted to include at least a metal layer that, when formed in conjunction with a via hole and contact, would provide overlap such that via misalignment does not result in poor contact between the via contact material and the landing pad material.

We find that, based on the foregoing claim interpretation, all of the claim elements of claim 1 are met by the combination of Nguyen and Nakamura as set forth by the examiner. Appellant argues that, "Flattening just the dielectric layer 40 surface above the transistors (12 and 20) of Nguyen et al. according to this alleged motivation is not the same as 'planarizing said

first barrier layer' as claimed." (Appeal Brief, page 8.) According to appellant's argument, planarizing only a portion of the dielectric layer **40** would not meet the claim term "planarizing," which requires making the entire dielectric layer planar. Appellant, however, does not point to any evidence that the ordinary meaning of "planarizing" is restricted to only creating a globally planar structure. We do not subscribe to appellant's interpretation of the claim term "planarizing" since there is nothing in the claim itself or in the specification that defines or otherwise restricts the broadest reasonable claim interpretation thereof in the manner suggested by appellant.

We turn now to appellant's challenge to the motivation for combining Nguyen with Nakamura found by the examiner. It is well settled that in order to establish that the claimed invention would have been obvious to a person of ordinary skill in the art at the time of the invention under 35 U.S.C. § 103(a), the examiner must show some objective teaching, suggestion, or motivation in the applied prior art or knowledge generally available to one of ordinary skill in the art that would have led that person to combine the teachings. *In re Rouffet*, 149 F.3d 1350, 1358, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998); *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d at 1266, 23 USPQ2d at 1784-85.

Appellant acknowledges the examiner's contention that "it is well known in the art [that] a flat surface provides better step coverage and the ability to use optical lithography for fabricating the ICs with submicron feature sizes." (Brief, page 8.) Appellant has not challenged the availability of this knowledge to a person of ordinary skill in the art. *See In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 421 (CCPA 1970) ("Where the appellant has failed to challenge a fact judicially noticed and it is clear that he has been amply apprised of such finding so as to have the opportunity to make such challenge, the board's finding will be considered

conclusive by this court."). Instead, appellant argues that, even assuming that this statement is true, a *prima facie* case has not been set forth. Specifically, appellant argues that "Nguyen et al. specifically teaches that a flat dielectric layer 40 is undesirable." (Appeal Brief, page 8.) We disagree. Appellant has not pointed out where Nguyen "specifically" teaches that a flat dielectric layer **40** would have been undesirable. Appellant's contention that Nguyen teaches away from "planarizing" appears to be based solely on the figures, which depict a non-planar layer **40**, and the bare fact that Nguyen does not teach global planarization. This is not the kind of teaching that would "teach away" in the sense of defeating obviousness since there is nothing that suggests that planarizing any portion of Nguyen would likely be unproductive of the claimed result. See *In re Gurley*, 27 F.3d 551, 552, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994) ("[A] reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant."). We find that nothing in Nguyen suggests that it is undesirable to planarize a portion of the dielectric layer **40** above the transistor gate.

Appellant further contends that applying Nakamura's teaching of reflow "would result in an absence of dielectric layer 40 covering the transistor structure 12 and 20 and may endanger the integrity of the transistor structures 12 and 20." (Appeal Brief, page 8.) Indeed, appellant goes so far as to state that "any planarization, or polishing, of the dielectric layer 40 of Nguyen et al. would necessarily result in the planarization of the covered structure down to the dielectric layer 40 surface." (Appeal Brief, page 9.) Both of the foregoing arguments result from appellant's incorrect understanding of the breadth of the term "planarizing." It suffices to say that the term "planarizing" as claimed does not require global planarization and thus one would not need to create an "absence of dielectric layer 40 covering the transistor structure 12 and 20" or "planarization of the covered structure down to the dielectric layer" before fully meeting the claimed "planarizing" limitation. Accordingly, we find no error in the combination of Nguyen with Nakamura under 35 U.S.C. § 103(a).

We now consider the grounds of rejection of claims 3 and 4 under 35 U.S.C. § 103(a)

based on Nguyen, Nakamura, and Maari and claim 6 under 35 U.S.C. § 103(a) based on Nguyen, Nakamura, and appellant's admitted prior art (Figs. 35-38, page 4, lines 26-29, and page 5, lines 1-5). We find that claims 3, 4, and 6 depend from claim 1 and incorporate the limitations of claim 1 by reference. We note that appellant does not provide separate arguments as to claims 3, 4, or 6 beyond the arguments directed to the ground of rejection of claim 1. Because we find that it was not improper to combine Nguyen with Nakamura under 35 U.S.C. § 103(a) we sustain the rejection of claims 3, 4, and 6 as well.

We now turn to the examiner's decision rejecting claims 8 and 9 over Nakamura, Takebuchi, and appellant's admitted prior art (Figs. 35-38, page 4, lines 26-29, and page 5, lines 1-5). The examiner admits that the limitation "planarizing said first barrier layer to expose said at least one transistor gate member" is not taught in Nakamura. (Answer, page 9.) Takebuchi is cited to overcome this deficiency in Nakamura. Takebuchi teaches planarizing a dielectric layer **6** down to the surface of the gate electrode **4** in order to improve contact resistance between the gate electrode **4** and a contact wiring layer **11** formed on the gate electrode (Takebuchi, **Fig. 1**). We do not see how it would be possible to planarize the dielectric layer **8** in Nakamura all of the way down to the surface of the gate electrodes **4** as would be required to meet the "to expose" limitation without destroying the adjacent conductor lines **6** which are elevationally above the gate electrodes **4** and would appear to be all but entirely removed before the planarization could "expose" the upper surface of the gate electrode. It is impermissible under 35 U.S.C. § 103(a) to combine references where the proposed modification would render the prior art unsatisfactory for its intended purpose. *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Accordingly, the rejection of claims 8 and 9 over Nakamura, Takebuchi, and appellant's admitted prior art (Figs. 35-38, page 4, lines 26-29, and page 5, lines 1-5) is reversed. All of the grounds of rejection that are applied to claims 9 through 11 and 14 through 17 are likewise reversed since each of these grounds rely on the propriety of the combination of Nakamura and Takebuchi in the manner asserted with respect to claim 8.

The examiner's decision is affirmed-in-part.

Other Issues

In the event of further prosecution of the appealed claims before the examiner, the examiner should consider the following issues. Nakamura, **Fig. 4**, shows a semiconductor substrate **1** with an active region **3**; a planar first barrier layer **8**; a first conductive plug **10** filling a first opening that reaches the active area (not labeled, opposite active area 3); a "wiring pad" (not labeled, but positioned between plug **10** and plug **13** in the same layer as first wiring layer **11**, see col. 9, ll. 59-60) that only covers a single contact plug **10**; a second planarized barrier layer **12** over the first barrier layer **8**; and a second conductive plug **13** filling a second opening that reaches the "wiring pad." The examiner finds (Answer, page 10) that Nakamura's element **11** corresponds to and meets the claimed "contact land" limitation. Insofar as the examiner is referring to Nakamura's "wiring pad," which is situated between plugs **10** and **13** in **Fig. 16**, we discern no error in this particular finding. Thus, it appears that Nakamura would apply to at least appealed claim 1 under 35 U.S.C. § 102(e).

Appeal No. 2003-1367
Application No. 09/640,237

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

| | | |
|-----------------------------|---|-----------------|
| Chung K. Pak |) | |
| Administrative Patent Judge |) | |
| |) | |
| |) | |
| |) | BOARD OF PATENT |
| Charles F. Warren |) | APPEALS AND |
| Administrative Patent Judge |) | INTERFERENCES |
| |) | |
| |) | |
| Thomas A. Waltz |) | |
| Administrative Patent Judge |) | |

Appeal No. 2003-1367
Application No. 09/640,237

CFW/JV/cam

Trask Britt
P. O. Box 2550
Salt Lake City, UT 84110