

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte FRANSISCUS W. SIJSTERMANS

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Appeal No. 2003-1430  
Application No. 09/414,458<sup>1</sup>

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ON BRIEF

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Before DIXON, SAADAT and MACDONALD, Administrative Patent Judges.  
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1-9, which are all of the claims pending in this application.

We reverse.

BACKGROUND

Appellant's invention is directed to a vector processor for executing vector instructions through conditional execution that

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<sup>1</sup> Application for patent filed October 7, 1999, which claims the foreign filing priority benefit under 35 U.S.C. § 119 of European Patent Office (EPO) Application No. 98203397.9, filed October 9, 1998.

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depends on a condition value. According to Appellant, performing normal (non-vector) operations requires a simple access mechanism to the registers which is undesirable to be modified for vector operations to write back vector components (specification, page 1). Appellant provides a multiplexer for each field which is controlled by the condition data for that field allowing for all fields of the result to be written back (specification, page 2).

Representative independent claim 1 is reproduced as follows:

1. A data processor which uses storage units that are subdivisible into predetermined fields for executing instructions that cause the data processor to handle numbers from respective ones of the fields separately, an instruction set of the processor comprising a conditioned assignment instruction with operand locations for addressing storage locations of a plurality of address storage units, the data processor being arranged to respond to the conditioned assignment instruction by executing a respective operation for each field in parallel, the respective operation for each particular field being conditioned by respective condition data for that particular field, characterized in that the data processor comprises for each particular field a respective multiplexer, controlled by condition data for that particular field, the multiplexer for each particular field having

a first and second input coupled to a respective port for receiving a content of that particular field in a first and second storage location addressed by a first and second one of the operand locations respectively, and

an output for supplying a multiplex output to that particular field in a result of the conditioned assignment instruction.

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The Examiner relies on the following reference in rejecting the claims:

Glass et al. (Glass)	5,881,257	March 9, 1999 (filed Oct. 8, 1996)
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Claims 1-9 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Glass.

We make reference to the answer (Paper No. 15, mailed February 11, 2003) for the Examiner's reasoning in support of the rejection, and to the appeal brief (Paper No. 14, filed January 6, 2003) for Appellant's arguments thereagainst.

#### OPINION

Appellant argues that the multiplexer arrangement of Glass is responsive to the Hi/Lo bit and size bit to switch appropriate halves of a selected register (brief, page 5). Appellant further points out that Glass fails to teach or suggest a multiplexer for each particular field for receiving a content of that particular field in a first and second storage location (*id.*). Appellant also contrasts the connection of each multiplexer to particular fields for receiving the contents of the source register and for supplying the multiplexed output of the claimed invention, as depicted in Figure 4 of the application, with Figure 4 of Glass

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where multiple input ports per MUX, instead of a respective port per MUX, is shown (id.).

In response to Appellant's arguments, the Examiner asserts that the claimed multiplexer also has multiple ports, as shown in an annotated copy of Appellant's Figure 4 and included in the answer as Attachment II, labeled as W3 and W4 and connected to multiplexer 44a (answer, page 10). The Examiner also points to an annotated copy of Figure 4 of Glass, included in the answer as Attachment I, to identify the upper input B from an upper port G as well as the lower input C from a lower port H as the claimed multiplexer inputs that are coupled to respective ports (id.).

Before addressing the Examiner's rejection based on prior art, it is essential that we understand the claimed subject matter and determine its scope. Accordingly, we will initially direct our attention to Appellants' claim 1 in order to determine its scope. Claim interpretation must begin with the language of the claim itself. See Smithkline Diagnostics, Inc. v. Helena Laboratories Corp., 859 F.2d 878, 882, 8 USPQ2d 1468, 1472 (Fed. Cir. 1988). See also Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999) ("The starting point for any claim construction must be the claims themselves.").

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A review of claim 1 reveals that for each particular field a respective multiplexer is provided which receives a content of that particular field associated with a first and a second storage location. Once the content of that field is multiplexed, the result is outputted to that particular field in an output which requires that each multiplexer receive a distinct content from a specific field. As shown in Figure 4, multiplexer 44a receives content of fields 41a and 43a on the left side of the input ports 40 and 42. Similarly, multiplexer 44b receives the content from fields 41b and 43b and so on while the results of each multiplexed field is sent to the corresponding fields 45a-45d of output port 46. Therefore, each multiplexer receives data only from a particular field and different from other multiplexers' fields. Independent claims 6 and 9 also require that the manipulation of the content data be performed with respect to each particular field.

A rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference. In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994). See also Atlas Powder Co. v. Ireco Inc., 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999).

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We observe that Glass, as depicted in the annotated copy of Figure 4 (Attachment I to the answer), discloses that each MUX receives a content of the same line (field) 16 (G or H) which is different from the claimed features. Glass actually discloses a multiplexer arrangement for switching appropriate halves of a selected register (col. 21, lines 32-36), and not for receiving a content of a particular field in two storage locations. Therefore, what the Examiner takes for different fields are, in fact the low and the high bits of a register, shown as sections I and H in the annotated copy of Figure 4 of Glass.

In view of the analysis above, we find that the Examiner has failed to meet the burden of providing a prima facie case of anticipation since, as discussed above, the multiplexers of Glass correspond to the same register content instead of each to a particular field. Accordingly, the rejection of claims 1-9 under 35 U.S.C. § 102 over Glass cannot be sustained.

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CONCLUSION

In view of the foregoing, the decision of the Examiner  
rejecting claims 1-9 under 35 U.S.C. § 102 is reversed.

REVERSED

JOSEPH L. DIXON	)	
Administrative Patent Judge	)	
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	)	BOARD OF PATENT
MAHSHID D. SAADAT	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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ALLEN R. MACDONALD	)	
Administrative Patent Judge	)	

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Philips Intellectual Property  
& Standards  
P.O. Box 3001  
Briarcliff Manor, NY 10510