The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte THOMAS J. WILSON

Appeal No. 2003-1965
Application 09/275,496

ON BRIEF

Before HAIRSTON, FLEMING, and SAADAT, **Administrative Patent Judges.**

FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 22, all the claims present in the instant application.

Invention

The invention relates to high speed digital communication systems. In particular, the invention relates specifically to high speed serial interface for ASIC to ASIC data transmissions.

See page 1 of Appellant's specification. There have been several attempts to solve the problem of maintaining phase coherence between the data transmitted from one ASIC to the same received at another ASIC when each ASIC has its own clock domain. See page 3 of Appellant's specification. Appellant solves this problem of ASIC-to-ASIC high speed data transmissions by providing: a transmitter and receiver operating within the same frequency and clock domain; a receiver that can sample data at n phase intervals; a mechanism for synchronizing this data to a common phase interval; a mechanism for analyzing the synchronizing data and subsequently determining one of the n phase intervals to be best fit and a mechanism for reconstructing n data packages from synchronized data that represent n data packets sampled at n phase intervals. See page 6 of Appellant's specification.

Referring to figure 1, an overall diagram of a high speed serial interface 10 is shown. The system comprises a transmitting ASIC 14, a receiving ASIC 16, and a reference clock 12 that drives both ASICs 14 and 16. See page 10 of Appellant's specification. Both transmitting ASIC 14 and the receiving ASIC 16 comprising PLL's 18 and 24 that receive reference clock signal 12 and allow their respective ASIC devices to operate at some

common frequency, Px. Since both PLL's 18 and 24 use the same reference clock, their frequencies will be the same but not necessarily in phase. The PLL's 18 and 24 also each generate additional clock signals that operate at a frequency of Bx. The PLL 24 within the receiving ASIC 16 generates n Bx clocks, each phased spaced within a Bx clock cycle as well as a receiver Px clock that will ultimately return data to the receiver ASIC 16 logic. Within the receiving ASIC 16, a receiver 26 receives and samples the data packet 22 at each of the n phase intervals in the Bx frequency domain, and on both edges of each n phase interval clocks. The samples 28 are synchronized to the Bx clock having a phase interval of 0 degrees and are then stored in a shift register 30 and analyzed to determine an initial phase relationship between the transmitted data packets and the receiver clock. If phase delay drifting has been detected, the receiver can compensate for the phase delay drifting by re-synchronizing the received data packets to the receiver clock phase. See page 11 of Appellant's specification.

The system also has a mechanism for storing a history of the synchronized data, using the results of the comparison analysis

to determine transmitter to receiver phase delay drift, and a mechanism for compensating for the identified phase delay drift. See pages 6 and 7 of Appellant's specification.

Referring to figures 4 through 6, a data packet collection scheme pursuant to Appellant's invention is depicted by utilizing six Bx clocks and six data paths. In figure 4, a timing diagram 34 shows a single Px clock signal (system clock) and six Bx clock signals identified as Bx0, Bx1, Bx2, Bx3, Bx4 and Bx5. As can be seen, each Bx clock is phase shifted by a 30 degree interval relative to the Bx0 clock signal. During operation, the data stream is sampled by each of the Bx clocks. The resulting sample is stored into the n=0 history buffer depicted in figure 5. At the subsequent five Bx clock intervals, it can be seen that data bit B is sampled. The results are stored in sequence history buffers (n=1, 2, 3, 4, and 5) as shown in figure 5. See page 22 of Appellant's specification. As can be seen in figures 4 and 5, the history buffers 38 could be examined to determine which of the n history buffers contain the BCDE signature. In this case, buffers n=1, 2, 3, 4, and 5 each contain the signature data packet. From those buffers that contain the signature, a middle one of the buffers could be selected to identify the "preferred" phase interval that represent the best fit among all of the six

clock intervals. See page 23 of Appellant's specification.

Independent claims 1 and 20 are representative of the Appellant's claimed invention and is reproduced as follows:

1. A system for receiving packets of serial data in relation to a system clock having a preselected frequency, comprising:

a mechanism for sampling each data packet at n clock intervals, wherein each of the n clock intervals is phase shifted in relation to the system clock, and wherein one of the n clock intervals is a preferred interval, and the remaining clock intervals are neighboring intervals; and

a mechanism for comparing the data packet sampled at the preferred interval with the data packet sampled at each of the neighboring intervals.

20. A receiver comprising:

a system clock;

a plurality of history buffers for receiving common data and each clocked by one of a plurality of sample clocks spaced at preselected regular intervals in relation to the system clock;

a monitoring means for monitoring a time relationship between common data received at the history buffers and the system clock;

a determining means for determining which one of the plurality of history buffers receives the common data in a most optimal time relationship with the system clock; and

an output means for selectively outputting the common data from one of the history buffers determined by the determining means to be receiving the common data in the most optimal time relationship with the system clock.

References

The reference relied on by the Examiner is as follows:

Buckner et al. (Buckner) 5,509,037 Apr. 16, 1996

Rejections at Issue

Claims 1 through 4, 9 through 12, and 16 through 21 stand rejected under 35 U.S.C. § 102 as being anticipated by Buckner.

Claims 5-8, 13-15, and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Buckner.

Throughout our opinion, we will make reference to the briefs[1] and answer for the respective details thereof.

OPINION

With full consideration being given to the subject matter on appeal, the Examiner's rejections and the arguments of Appellant and Examiner, for the reason stated **infra**, we reverse the Examiner's rejection of claims 1 through 4, 9 through 12 and 16 through 21 under 35 U.S.C. § 102 and we reverse the Examiner's rejection of claims 5 through 8, 13 through 15 and 22 under 35 U.S.C. § 103.

---

[1] Appellant filed an appeal brief on January 22, 2003. Appellant file a reply brief on May 20, 2003. The Examiner mailed an office communication on July 14, 2003, stating that the reply brief has been entered into the records.

For claims 1 through 4 and 9 through 12, Appellant argues that Buckner does not teach “a mechanism for comparing the data packet sampled at preferred interval with the data packet sampled at each of the neighboring intervals” as recited by independent claim 1. See pages 7 through 16 of Appellant’s brief.

For claims 16 through 19, Appellant argues that Buckner does not teach “comparing data in the preferred data path with data in each of the neighboring paths” as recited in independent claim 16. See pages 17 through 20 of Appellant’s brief.

“Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention.” **RCA Corp. v. Applied Digital Data Sys, Inc.** 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.), cert. dismissed, 468 U.S. 1228 (1984), **citing Kalman v. Kimberly-Clark Corp.,** 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983).

The Examiner argues that Buckner teaches in figure 6a a comparison of each of the phases. See page 4 of the Examiner’s answer.

Appellant argues that claims 1 through 4, 9 through 12 and 16 through 19 require that the data packets sampled at each of

the clock signal phases θ_2, θ_3, θ_4 and θ_5 be compared with the data packets sampled at the clock phase θ_1. Appellant argues that Buckner shows in figure 6a and explains in column 4, lines 51 through column 5, line 3 that only data packets sampled at θ_2 and θ_5 are compared with data packets sampled at θ_1. Thus, Buckner does not teach "comparing the data packet sampled at preferred intervals with data packet sampled at each of the neighboring intervals" as required by the claims. See page 2 of Appellant's reply brief.

Upon our review of Buckner, we find that Buckner does teach that the data signal DATA-IN clocked by θ_1 and θ_2 are compared. Furthermore, we find that Buckner teaches that the data signal DATA-IN clocked by θ_5 and θ_1 are compared. However, we fail to find that Buckner teaches that θ_1 is compared with θ_3 and θ_4. See Buckner, figure 6a and column 4, line 51 through column 5, line 3. Therefore, we will not sustain the Examiner's rejection of claims 1 through 4, 9 through 12 and 16 through 19 under 35 U.S.C. § 102.

For claims 20 through 21, Appellant argues that Buckner does not teach "a monitoring system for monitoring a time relationship between common data received at the history buffers and the system clock." In particular, Appellant argues that the

Examiner's reliance on Buckner's history buffer fails to show preforming a monitoring function as required by claim 20. In particular, Appellant argues that the term monitoring means to keep track of. Appellant argues that Buckner's history buffer align but does not perform monitoring. Upon our review of Buckner, we agree with the Appellant that the Examiner has not shown a **prima facie** case of showing that Buckner teaches "a monitoring system for monitoring a time relationship between common data received at the history buffers and the system clock" as required by Appellant's claims 20 and 21. Therefore, we will not sustain the Examiner's rejection of these claims under 35 U.S.C. § 102.

For the rejection of claims 5 through 8, 13 through 15 and 22 under 35 U.S.C. § 103 as being unpatentable over Buckner, we note that the Examiner relies on the above reasoning for this rejection as well. Therefore, we will not sustain this rejection for the same reasons.

In view of the foregoing, we have not sustained the Examiner's rejection of claims 1 through 4, 9 through 12 and 16 through 21 under 35 U.S.C. § 102 and we have not sustained the Examiner's rejection of claims 5 through 8, 13 through 15 and 22 under 35 U.S.C. § 103.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
MAHSHID SAADAT Administrative Patent Judge	)	

MRF:pgc

Arlen L. Olsen
Schmeiser, Olsen & Watts
3 Lear Jet Lane
Suite 201
Latham, NY 12110