

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHAU-LIN SHUE and MEI-YUN WANG

Appeal No. 2003-1971
Application No. 09/489,970

ON BRIEF

Before HAIRSTON, FLEMING, and LEVY, ***Administrative Patent Judges.***
FLEMING, ***Administrative Patent Judge.***

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1, 2, 9, 12 and 13. Claims 3-8, 10 and 11 stand objected to for being dependent on a rejected claim. Claim 14 has been allowed. Thus, the only claims before us for our consideration are claims 1, 2, 9, 12 and 13.

Invention

The invention relates to the fabrication of integrated circuit devices. In particular, the invention relates to a method of forming salicided gate electrodes whereby no danger exists of having an electrical short between the gate contact and

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the contacts for the source and drain regions. See page 1 of Appellants' specification.

Referring now to specifically Figure 4, there is shown a cross section of a partially completed gate electrode 40 on a substrate 10. See page 15 of Appellants' specification. Figure 5 shows a cross section of a gate electrode 40 whereby gate spacers of oxide (42) have been created. The layer 42 forms the first layer of a double layer gate spacer on the side walls of the partially completed gate of electrode 40. See page 16 of Appellants' specification. Figure 6 shows a cross section of the gate electrode after the second layer 44 of silicon nitride has been created to form the second layer of the gate spacers. See pages 17 and 18 of Appellants' specification. Figure 7 shows a cross section of the gate electrode after the source 52 and drain 54 are implanted into the surface of substrate 10. See page 19 of Appellants' specification. Figure 8 shows a cross section of the gate electrode after the layer 46 of the cobalt has been deposited over the surface of the structure 40. See page 19 of Appellants' specification. Figure 9 shows the siliciding of the layer of cobalt creating reacted layers 56, 58 and 60 and unreacted layer 46 of cobalt. See page 20 of Appellants' specification. Figure 10 shows a cross section of the gate

structure of the invention after the removal of the unreacted cobalt. See page 21 of Appellants' specification. Figure 11 shows a cross section of the gate structure after the removal of the outer gate spacer layer 44. See pages 21 and 22 of Appellants' specification.

Independent claim 1 is representative of Appellants' claimed invention and is reproduced as follows:

1. A method for manufacturing salicided regions for electrical contact to a semiconductor device, comprising the sequential steps of:

providing a silicon semiconductor substrate whereby said substrate has been provided with a semiconductor device whereby said semiconductor device is a partially completed gate electrode structure;

creating double layered gate spacers on the sidewalls of said partially completed gate electrode structure said double layered gate spacers containing an inner gate spacer comprising oxide layer that is immediately adjacent to and overlying the sidewalls of said partially completed gate electrode structure and an outer gate spacer layer comprising silicon nitride that overlays said inner layer thereby creating an intermediately completed gate electrode structure;

performing source and drain implants into the surface of said substrate whereby said source and drain implants are self-aligned with said intermediately completed gate electrode structure;

depositing a layer of cobalt over the surface of said substrate thereby including the surface of said intermediately completed gate electrode structure;

saliciding said layer of cobalt thereby creating reacted and unreacted layers of cobalt on the surface of said substrate

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thereby including the surface of said intermediately completed gate electrode structure;

removing said unreacted cobalt from the surface of said substrate thereby including the surface of said intermediately completed gate electrode structure; and

removing said outer gate spacer layer from said intermediately completed gate electrode structure, using a warm H₃PO₄ based etchant, thereby creating a gate electrode structure.

References

The references relied on by the Examiner are as follows:

Tsai et al. (Tsai '024)	5,668,024	Sep. 16, 1997
Tsai et al. (Tsai '890)	5,851,890	Dec. 22, 1998
DeBoer et al. (DeBoer)	6,258,729	Jul. 10, 2001

Rejection at Issue

Claims 1, 2, 9, 12 and 13 stand rejected under 35 U.S.C. § 103 as being unpatentable over Tsai '890, Tsai '024 and DeBoer '729.

OPINION

With full consideration being given to the subject matter on appeal, the Examiner's rejection and arguments of Appellants and Examiner, for the reasons stated *infra*, we affirm the Examiner's rejection of claims 1, 2, 9, 12 and 13 under 35 U.S.C. § 103.

At the outset, we note that Appellants state on page 11 of the brief that claim 1 and dependent claims 2-13 form a first group of claims. 37 CFR § 1.192 (c)(7) (July 1, 2002) **as**

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amended at 62 Fed. Reg. 53196 (October 10, 1997), which was controlling at the time of Appellants filing the brief, states:

For each ground of rejection which [Appellants contest and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, Appellants explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

We will, thereby, consider Appellants' claims as standing or falling together and we will treat claim 1 as a representative claim of that group. **See In re McDaniel**, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002) ("If the brief fails to meet either requirement [of 37 CFR § 1.192(c)(7)], the Board is free to select a single claim from each group of claims subject to a common ground of rejection as representative of all claims in that group and to decide the appeal of that rejection based solely on the selected representative claim.") **See also, In re Watts**, 354 F.3d 1362, 1368, 69 USPQ2d 1453, 1458 (Fed. Cir. 2004).

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a **prima facie** case of

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obviousness. ***In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). ***See also In re Piasecki***, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. ***In re Fine***, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. ***Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444. ***See also Piasecki***, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." ***Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." ***In re Lee***,

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277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). With these principles in mind, we commence review of the pertinent evidence and arguments of Appellants and Examiner.

Appellants point out that claim 1 recites that the oxide is used for a first gate spacer and that silicon nitride is used for a second gate spacer. Appellants argue that Tsai '890 claims a composite spacer comprising silicide which has no commonality with the instant invention.

The question is not what Tsai '890 claims but instead what Tsai '890 teaches. Tsai '890 teaches a double layer gate spacer on the sidewalls of the partially completed gate electrode structure, said double layer gate spacer containing an inner gate spacer 50 comprising an oxide layer that is immediately adjacent to and overlying the sidewalls of the partially completed gate electrode structure and outer gate spacer layers 60 and 62 comprising silicon nitride that overlays said inner layer thereby creating an intermediate completed gate electrode structure as recited in Appellants' claim 1. See Tsai '890, column 4, line 50 through column 5, line 17. Therefore, Tsai '890 does teach that the oxide is used for a first gate spacer and that silicon nitride is used for a second gate spacer.

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Appellants concede that Tsai '024 does teach the removal of the second spacer. However, Appellants argue that the process used is prone to damaging the formed silicide cobalt.

While this court indeed warns against employing hindsight, its counsel is just that--a warning. That warning does not provide a rule of law that express, written motivation to combine must appear in prior art references before a finding of obviousness. Stated differently, this court has consistently stated that a court or examiner may find a motivation to combine prior art references in the nature of the problem to be solved. **Ruiz v. A.B. Chance Co.**, 357 F.3d 1270, 1276, 69 USPQ2d 1686, 1690 (Fed. Cir. 2004). **Also see Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.**, 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630 (Fed. Cir. 1996); **Display Techs. Inc. v. Paul Flum Ideas, Inc.**, 282 F.3d 1340, 1346-47 (Fed. Cir. 2002); **In re Huang**, 100 F.3d 135, 139, 40 USPQ2d 1685, 1689 (Fed. Cir. 1996).

Upon our review of Tsai '024, we fail to find any teaching that the removal process disclosed would damage the silicide cobalt layer. Furthermore, Tsai '024 suggests that silicon nitride can be removed with hot phosphoric acid. See Tsai '024, column 4, lines 2-4. DeBoer also teaches the use of an APM

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solution as well as a hot phosphoric solution to remove insulating layers. See DeBoer, column 11, lines 25-40. Therefore, one of ordinary skill in the art would have had before him these teachings that would lead him to use a hot phosphoric solution to remove the silicon nitride spacer as claimed.

Appellants have not made any other arguments as to the claims. 37 CFR § 1.192(a) states:

Appellants must, within two months from the date of the notice of appeal under § 1.191 or within the time allowed for reply to the action from which the appeal was taken, if such time is later, file a brief in triplicate. The brief must be accompanied by the fee set forth in § 1.17(c) and must set forth the authorities and arguments on which [A]ppellants will rely to maintain the appeal. Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences, unless good cause is shown.

Thus, 37 CFR § 1.192 provides that only the arguments made by Appellants in the brief will be considered and that failure to make an argument constitutes a waiver on that particular point. Support for this rule has been demonstrated by our reviewing court in *In re Berger*, 279 F.3d 975, 984, 61 USPQ2d 1523, 1528-29 (Fed. Cir. 2002), wherein the Federal Circuit Court stated that because the Appellants did not contest the merits of the rejections in the brief to the Federal Circuit Court, the issue is waived.

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In view of the foregoing, we have sustained the Examiner's rejection of claims 1, 2, 9, 12 and 13 under 35 U.S.C. § 103.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
MICHAEL R. FLEMING)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
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