The opinion in support of the decision being entered today was ***not*** written for publication and is ***not*** binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HUI-LING LOU,
GERALD DIETRICH THOMAS SCHULLER
and
VIJITHA WEERACKODY

Appeal No. 2003-2038
Application No. 09/288,833

ON BRIEF

Before JERRY SMITH, FLEMING, and RUGGIERO, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 20, all the claims pending in the instant application.

Invention

The invention relates to audio and video streaming applications employed in data packet-based networks such as, for example, the Internet. Internet applications that employ audio and video streaming are becoming increasingly prevalent. As a natural consequence, there are large packet delays. Also, data packets are sometimes even lost completely by the network. Buffering helps to reduce the detrimental effects of the relatively large and variable packet delays which result from varying levels of network congestion. Packet losses in the network are typically addressed by using a forward error correction code across the packets. See page 1 of Appellants' specification. Clearly then, a large receive buffer is highly desirable to provide a better quality signal because it increases the probability that most of the packets representing data within a given period of time will have been successfully accumulated in the buffer before it is necessary to decode them for playback. However, a large buffer also results in large buffering delays. It would be desirable, therefore, to provide a source coding and receive data buffering scheme which results in more acceptable

buffering delays without sacrificing the benefits of using a large receive buffer. See page 2 of Appellant's specification.

Figure 1 shows an illustrative embodiment of Appellants' invention. In particular, the figure shows a program source which is encoded by both source coder 11 and source coder 12 to produce two independent bit streams. See page 5 of Appellants' specification. The signal generated by source coder 12 is delayed prior to transmission by a conventional delay element 14. The amount of delay which is applied is approximately equal to the difference in the delays which are to be incurred by the receive buffers used at the receiver prior to the decoding of the two data streams. Channel 16 represents a communications channel adapted to transmission of packet-based data streams such as the Internet. See page 6 of Appellants' specification. The receiving end of channel 16 comprises two receive buffers 17 and 18. Receive buffer 17 has an associated buffer delay of n_1 and receive buffer 18 has an associated buffer delay of n_2. In accordance with the principles of the invention, n_1 is greater than n_2. Receive buffer 17 and receive buffer 18 are used to provide input to decoder 21 and decoder 22,

respectively. See page 7 of Appellants' specification. Selection processor 24 selects either the output of decoder 21 or the output of decoder 22. The output of decoder 22 is initially selected by selection processor 24. After the time period delay provided by delay element 14 has elapsed and once delay n_1 has elapsed, the output of decoder 21 is selected. See page 8 of Appellants' specification.

Appellants' claim 1 is representative of Appellants' claimed invention and is reproduced as follows:

> 1. A method of processing two or more sequences of data packets received from a network, each of said sequences of data packets representing a common program source, the method comprising the steps of:
>
> buffering data packets comprised in a first one of said sequences in a first receive buffer having a first buffering delay;
>
> buffering data packets comprised in a second one of said sequences in a second receive buffer having a second buffering delay, wherein said second buffering delay is smaller then said first buffering delay;
>
> decoding the data packets buffered in said second receive buffer after said second buffering delay has elapsed;
>
> decoding the data packets buffered in said first receive buffer after said first buffering delay has elapsed;

> generating a reproduction of said program source based at least upon the decoding of the data packets buffered in said second receive buffer before said first buffering delay has elapsed, and based at least upon the decoding of the data packets buffered in said first receive buffer after said first buffering delay has elapsed.

References

The references relied on by the Examiner are as follows:

Cellario et al. (Cellario)	6,108,626	Aug. 22, 2000 (filed May 14, 1998)
Goyal et al. (Goyal)	6,345,125	Feb. 5, 2002 (filed Feb. 25, 1998)
Adams (European Patent Application)	0,695,094	Jan. 31, 1996

Orchard et al. (Orchard), "Redundancy Rate-Distortion Analysis of Multiple Description Coding Using Pairwise Correlating Transforms," IEEE, 1997

Rejections at Issue

Claims 1, 3 through 7, 9 through 11, 13 through 17, 19 and 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Cellario. Claims 2 and 12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Adams in view of Cellario and Goyal. Claims 8 and 18 stand rejected under

35 U.S.C. § 103 as being unpatentable over Adams in view of Cellario and Orchard.

Throughout our opinion, we will make reference to the briefs[1] and the answer for the respective details thereof.

OPINION

With full consideration being given to the subject matter on appeal, the Examiner's rejections and the arguments of Appellants and the Examiner, for the reasons stated ***infra***, we reverse the Examiner's rejection of claims 1 through 20 under 35 U.S.C. § 103.

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a ***prima facie*** case of obviousness. ***In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). ***See also In re Piasecki***, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in

[1] Appellants filed an appeal brief on February 19, 2003. Appellants filed a reply brief on June 25, 2003. The Examiner mailed out an Office communication on July 18, 2003 stating that the reply brief has been entered.

the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. ***In re Fine***, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. ***Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444. ***See also Piasecki***, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." ***Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." ***In re Lee***, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). With these principles in mind, we commence review of the pertinent evidence and arguments of Appellants and Examiner.

Appellants argue that the combination of Adams and Cellario fails to teach or suggest all the limitations set forth

in independent claims 1 and 11. Specifically, Appellants argue that Adams and Cellario fail to teach or suggest "processing two or more sequences of data packets . . . , each of said sequence of data packets representing a common program source" as required by claims 1 and 11. Appellants further argue that the combination of Adams and Cellario fails to teach or suggest "buffering data packets comprised in a second one of said sequences in a second receive buffer having a second buffering delay, wherein said second buffer delay is smaller than said first buffering delay," as recited in Appellants' claim 1. Appellants further argue that the combination of Adams and Cellario fails to teach or suggest "a second receive buffer having a second buffering delay for buffering data packets comprised in a second one of said sequences, wherein said second buffering delay is smaller than said first buffering delay" as recited in Appellants' claim 11. See pages 8 through 10 of Appellants' brief.

In response, the Examiner argues that the combination of Adams and Cellario teaches buffering data packets comprising a second one of said sequences in a second receive buffer having a second buffering delay, wherein said second buffering delay is

smaller than the first buffering delay. The Examiner points out that Adams teaches multiple video data streams that are received and decoded simultaneously using multiple buffers and decoder servers. The Examiner points out that Cellario teaches multiple audio data streams from the same program source which could be saved in multiple buffers. The Examiner argues that Adams uses an input switch to control the flow rates of the two video data streams on the two video lines. The first video data stream flows at a first rate. The second video data stream flows at a second rate, which could be different than the first one. The Examiner points us to Adams, column 3, lines 20-29. See page 18 of the Examiner's answer.

In the reply brief, Appellants argue that Adams and Cellario fail to teach or suggest buffering data packets from one of the sequences of a first receive buffer having a first buffering delay and buffering data packets from another one of the sequences in a second receive buffer having a second buffering delay, the second buffering delay being smaller than the first buffering delay, as set forth in claims 1 and 11. Appellants point out that with reference to figure 3, Adams discloses a video decompression system 100 that includes two

parallel video compression circuits 120 and 130. Adams clearly intends that the two decompression circuits 120 and 130 comprise buffers that are identical to one another. Appellants argue that Adams does not teach or remotely suggest that the buffers are of unequal size or that they have different buffering delays associated therewith as required by Appellants' claims. See Appellants' Reply Brief, pages 3 and 4.

We note that the Examiner has not been able to point to the specific teaching in either Adams or Cellario that teaches buffering data packets from one of the sequences in a first receive buffer having a first buffering delay and buffering data packets from another one of the sequences in a second receive buffer having a second buffering delay, the second buffering delay being smaller than the first buffering delay as required by Appellants' claims. Furthermore, we note that Adams teaches that the buffers comprise eight 256K words by 16 bit dynamic random access memories coupled to the decoder. See Adams, column 5, lines 3-6. Therefore, Adams teaches that the buffers are identical and therefore would have the same buffering delays, not different as required by the claims.

Turning to the rejection of claims 2 and 12 as being unpatentable over Adams in view of Cellario and Goyal, and the rejection of claims 8 and 18 as being unpatentable over Adams in view of Cellario and Orchard, we fail to find that Goyal or Orchard teaches the above limitation. We note that claims 2, 8, 12 and 18 depend from claims 1 and 11. Therefore, we will not sustain these rejections for the same reasons as above.

In view of the foregoing, we have not sustained the Examiner's rejection of claims 1 through 20 under 35 U.S.C. § 103.

REVERSED

JERRY SMITH Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JOSEPH F. RUGGIERO Administrative Patent Judge	)	

MRF:psb

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