

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 39

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHAN-DONG CHO

Appeal No. 2003-2108
Application No. 08/881,123

ON BRIEF

Before HAIRSTON, MARTIN, and BARRY, Administrative Patent Judges.
HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 2 and 5 through 20. Claims 3 and 4 are directed to allowable subject matter.

The disclosed invention relates to a method and apparatus for controlling the access of a plurality of devices to a memory based upon a predetermined priority order of the devices.

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Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. An apparatus having a memory controller for controlling access to a memory by a plurality of devices, the apparatus comprising:

a priority order controller

to generate either

an acknowledgment signal to a corresponding one of the plurality of devices in response to a request signal generated by the corresponding device, or

the acknowledgment signal to the corresponding device according to a predetermined priority order if more than one request signal is simultaneously generated from the plurality of devices, and

to subsequently deactivate the generated acknowledgment signal if an access actuation signal is deactivated,

wherein the access actuation signal is distinct from the request signal and is issued by the memory controller to indicate that one of the plurality of devices is accessing the memory.

The reference relied on by the examiner is:

Craft et al. (Craft) 5,438,666 Aug. 1, 1995

Claims 1, 2 and 5 through 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Craft.

Reference is made to the briefs (paper numbers 31 and 34) and the answer (paper number 32) for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the anticipation rejection of claims 1, 2 and 5 through 20.

We agree with the examiner (answer, pages 3 and 4) that Craft discloses (Figures 4 and 5) a computer system 300 with a shared address, data and control bus 318 that provides access to a memory 314 and a bus arbitration control circuit 370 that determines which of a plurality of devices 344, 348, 360, 362 or 364 is granted access to the shared bus based on priority, and generates "either an acknowledgment signal to a corresponding one of the plurality of devices in response to a request generated by the corresponding device, or the acknowledgment to the corresponding device according to a predetermined priority order if more than one request signal is simultaneously generated from the plurality of devices (see Fig. 4, bus arbitration control circuit 370; BUS MASTER A[,] 350 BUS MASTER B[,] 352 BUS MASTER C 354; and the respective bus grant lines, as acknowledge signal for the respective BUS MASTER; col. 11, lines 28-39; col. 14, line 26 to col. 15, line 60)." The bus arbitration control circuit 370 subsequently deactivates "the generated acknowledgment signal if an access actuation signal is

deactivated (see col. 14, lines 43-54), here for example, see Fig. 4, . . . and the deactivation of the DMA grant signal on the DMA grant line 374B when the DMA controller 340, that controls the floppy disk controller 344, deactivates the DMA request line on the DMA request line 374A to indicate to the bus arbitration control circuit 370 that the DMA operation is completed." We additionally agree with the examiner (answer, page 4) that "the access actuation signal is different from the request signal "

Based upon the foregoing, appellant argues (brief, page 8) that the examiner has attributed the functions of both the claimed priority controller and the memory controller to the bus arbitration control circuit 370. In response, the examiner agrees (answer, page 9) that "the DMA grant signal generated by the bus arbitration control circuit 370 in response to the DMA request to the bus arbitration control circuit 370, serves both as the DMA ACKNOWLEDGMENT signal and ACCESS ACTUATION signal."

If each grant output signal from the bus arbitration control circuit 370 in Craft functions as both an acknowledgment signal and an access signal, then we agree with the appellant's arguments (brief, page 9; reply brief, page 3) that a grant output signal from the bus arbitration control circuit 370 is

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never outputted to "subsequently deactivate the generated acknowledgment signal if an access actuation signal is deactivated" (claims 1 and 15). For this reason, the anticipation rejection of claims 1 and 15 is reversed.

Turning to claim 2, if the acknowledgment signal and the access request signal in Craft are the same signal, then we agree with the appellant's arguments (brief, page 10; reply brief, pages 4 and 5) that Craft can not "generate and transmit the access request signal to said memory controller in response to the generation of the corresponding acknowledgment signal." Thus, the anticipation rejection of claim 2 is reversed.

The anticipation rejection of claim 5 is reversed because we agree with the appellant's arguments (brief, pages 11 and 12; reply brief, pages 5 and 6) that Craft does not disclose "deactivating the acknowledgment signal after the access actuation signal is deactivated" because the two noted signals are a combined signal in Craft.

The anticipation rejection of claims 6, 16 and 17 is reversed because Craft does not disclose activating an acknowledgment signal after generating an access actuation signal (brief, pages 11 and 12). As indicated supra, the two signals are combined into a single signal in Craft.

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The anticipation rejection of claims 7 through 12, 18 and 19 is reversed because Craft does not deactivate "the acknowledgment signal upon the deactivation of the access actuation signal" (brief, page 9). As indicated supra, the two signals are a single signal in Craft, and are deactivated in unison.

The anticipation rejection of claim 13 is reversed because Craft does not "subsequently deactivate the generated acknowledgment signal if the access actuation signal is deactivated."

The anticipation rejection of claims 14 and 20 is reversed because Craft does not "generate and transmit the access request signal to said memory controller in response to the generation of the corresponding acknowledgment signal."

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DECISION

The decision of the examiner rejecting claims 1, 2 and 5 through 20 under 35 U.S.C. § 102(b) is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
JOHN C. MARTIN)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
)	
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LANCE LEONARD BARRY)	
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KWH/hh

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