

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No.12

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEFFREY L. DEENEY

Appeal No. 2003-2174
Application No. 09/915,071

ON BRIEF

Before WALTZ, TIMM, and JEFFREY T. SMITH, *Administrative Patent Judges*.
JEFFREY T. SMITH, *Administrative Patent Judge*.

DECISION ON APPEAL

Applicant appeals the decision of the Primary Examiner finally rejecting claims 1 to 13, all of the pending claims in the application. We have jurisdiction under 35 U.S.C. § 134.¹

¹ In rendering this decision, we have considered Appellants' arguments presented in the Brief filed December 19, 2002.

BACKGROUND

The invention relates to a semiconductor die comprising a pair of opposed parallel major surfaces and a periphery. The semiconductor die comprises an active circuit area within the boundary on one of the major surfaces. The active circuit area comprises at least one active circuit element that dissipates heat during operation. The semiconductor die comprises a heat spreading extension disposed between at least a portion of the boundary and at least a portion of the die periphery adjacent the boundary portion. The extension operates to establish a heat flow path to conduct heat away from the heat dissipating active circuit element. Claims 1 and 8, which are representative of the claimed invention, appear below:

1. A semiconductor die comprising:

a pair of opposed parallel major surfaces and a periphery;

an active circuit area within a boundary on at least one of the major surfaces of the semiconductor die, said active circuit area comprising at least one active circuit element that dissipates heat during operation; and

a heat spreading extension disposed between at least a portion of said boundary and at least a portion of said die periphery adjacent said boundary portion, said extension being operable to establish a heat flow path to conduct heat away from said at least one heat dissipating active circuit element.

8. A semiconductor package comprising:

a package substrate having an upper surface;

a thermally conductive cover secured to said package substrate, said cover including an inner surface, said inner surface of said cover and said upper surface of said package substrate defining a space; and

a semiconductor die enclosed within said space, said semiconductor die having a major surface and a periphery, said surface of said semiconductor die including an active circuit area comprising at least one active circuit element dissipating heat during operation of the semiconductor package, said active circuit area having a boundary, said surface of said semiconductor die being thermally coupled to said inner surface of said cover and wherein the die includes a heat spreading extension integral with the die, said heat spreading extension being disposed between said boundary of said active circuit area and said periphery of said die, said heat spreading extension being operable to establish a heat flow path to conduct heat away from said at least one active circuit element.

CITED PRIOR ART

As evidence of unpatentability, the Examiner relies on the following references:

Torres et al. (Torres)	5,962,926	Oct. 05, 1999
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The Examiner also relied on the admitted prior art of Figure 1.

The Examiner has rejected claims 1 to 7 as anticipated under 35 U.S.C. § 102(b) over Torres; and claims 8 to 13 as obvious under 35 U.S.C. § 103(a) over the combination of Torres and the admitted prior art of Figure 1. (Answer, pp. 3 to 13).

Appellant has indicated, Brief page 4, that claims 1, 2 and 3 stand or fall together, claim 4 stands or falls alone, claims 5 to 7 stand or fall together and claims 8 to 13 stand or fall together. We will consider the claims separately only to the extent that separate

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arguments are of record in this appeal. Note *In re King*, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); *In re Sernaker*, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983); 37 CFR § 1.192(c)(7)(2001).

DISCUSSION

We have carefully reviewed the claims, specification and applied prior art, including all of the arguments advanced by both the Examiner and Appellant in support of their respective positions. This review leads us to conclude that the Examiner's rejection of claims 1 to 7 under § 102(b) is well founded. We also conclude that the rejection of claims 8 to 13 under § 103(a) is well founded.

The rejection under § 102

The Examiner has found that Torres discloses a semiconductor die that anticipates the subject matter of claims 1 to 7. (Answer, pp. 4-8). We affirm primarily for the reasons advanced by the Examiner and add the following primarily for emphasis.

Appellant argues that Torres does not teach “an active surface. . . comprising at least one active circuit element that dissipates heat during operation.” (Brief, p. 7). We agree with the Examiner, Answer pages 11-12, that Torres discloses an active surface that implements application logic. The Examiner asserts that the active circuit element of Torres dissipates heat during operation. Appellant has not presented arguments or evidence to the contrary in supplemental briefing.

Appellant argues that the Examiner (Final Rejection p. 4) has dismissed claim language that is integral to the structural elements. (Brief, p. 7) We do not find Appellant's argument persuasive. The Examiner has responded to Appellant's argument in the Final Rejection, pages 7-8, and in the Answer, page 12. Appellant, in the Brief, has not addressed the Examiner's position from the Final Rejection. Appellant also has not presented arguments or evidence in rebuttal to the Examiner's position in supplemental briefing. Moreover, we agree with the Examiner that Torres discloses all of the structural elements of the claimed invention. As stated above, Torres' active circuit dissipates heat during operation. The extension around the active circuit area would function as a path away for heat to travel from the active circuit.

Appellant also argues that "Torres does not disclose or even suggest the location of any active circuit element, let alone one that is 'adjacent' to an active circuit area boundary." (Brief, p. 8). This argument is not persuasive. Torres describes an active circuit area (22) is surrounded by the periphery (24). Thus, Torres describes all of the elements of this claim.

Appellant's arguments with respect to claim 5 have been addressed by the Examiner in the Answer. (Pages 12-13). Moreover, as stated above, the Examiner asserted that Torres discloses an active surface that implements application logic which dissipates heat during

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operation. Appellant has not presented arguments or evidence to the contrary in supplemental briefing.

The rejection under § 103

The Examiner rejected claims 8 to 13 under 35 U.S.C. § 103(a) as obvious over the combination of Torres and the admitted prior art of Figure 1. (Answer, pp. 8-10). We affirm primarily for the reasons advanced by the Examiner and add the following primarily for emphasis.

Appellant argues that Torres does not teach the heat spreading extension that is required for claims 8-13. We do not agree. As stated by the Examiner, Torres discloses area (24) that does not contain active circuits. This area surrounds the active circuit. Thus, heat created in the active circuit area will spread to the non-active area.

Appellant argues that the object of Torres is to reduce the die area and fails to teach any temperature issues. (Brief, p. 11). Appellant's argument is not persuasive. There is no indication on this record that the size of the die area would prevent heat from spreading to a surrounding area. The Examiner's position that active circuits when functioning produce heat appears reasonable and has not been persuasively refuted by the Appellant. Appellant's representative's argument to the contrary is not persuasive. Unsupported arguments of counsel simply cannot take the place of evidence. *See In re Pearson*, 494 F.2d 1399, 1405,

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181 USPQ 641, 646 (CCPA 1974). Appellant has not presented evidence that the active area of a semiconductor functions at a lower temperature than the surrounding area that lacks active regions.

Based on our consideration of the totality of the record before us, having evaluated the *prima facie* case of obviousness in view of Appellant's arguments, we conclude that the subject matter of claims 8-13 would have been obvious to a person of ordinary skill in the art from the combined teachings of the cited prior art for the reasons stated above and in the Answer.

CONCLUSION

The rejection of claims 1-7 under § 102(b) over Torres is affirmed. The rejection of claims 8-13 under § 103(a) over the combination of Torres and the admitted prior art of Figure 1 is affirmed.

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Time for taking action

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

THOMAS A. WALTZ
Administrative Patent Judge

CATHERINE TIMM
Administrative Patent Judge

JEFFREY T. SMITH
Administrative Patent Judge

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