

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GEORGE JONATHAN KLUTH

Appeal No. 2003-2175
Application No. 09/712,234

ON BRIEF

Before KIMLIN, PAK, and POTEATE Administrative Patent Judges.
PAK, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1 through 11 and 13 through 24. Claim 25, the only other claim in this application, stands withdrawn from consideration by the examiner as being directed to a non-elected invention.

Appeal No. 2003-2175
Application No. 09/712,234

The subject matter on appeal is directed to a process for manufacturing a semiconductor device. Further details of this process are provided in representative claim 1 which is reproduced below:

1. A method of manufacturing a semiconductor device, the method comprising:

providing a silicon-containing semiconductor substrate, having an upper surface, comprising: a gate electrode formed on the substrate upper surface with a gate insulating layer therebetween, the gate electrode having an upper surface and opposing side surfaces;

amorphizing selected regions of the semiconductor substrate;

forming source/drain regions by doping the selected regions of the semiconductor substrate with a dopant;

depositing a metal layer over the semiconductor substrate; and

annealing the semiconductor substrate, wherein said metal layer is exposed, with a single heating step at a temperature of about 350°C to less than about 850°C for about 30 seconds to 60 minutes, to simultaneously activate the source/drain regions and to react the metal layer with underlying silicon in the gate electrode and source/drain regions to form metal silicide contacts.

The examiner relies on the following prior art references:

Chong et al. (Chong)	6,335,253	Jan. 01, 2002 (Filed Jul. 12, 2000)
Yamazaki et al. (Yamazaki)	0,011,598	Jan. 31, 2002 (Filed Aug. 27, 2001)

Appeal No. 2003-2175
Application No. 09/712,234

Claims 1 through 11 and 13 through 24 stand rejected under 35 U.S.C. § 103 as unpatentable over the combined disclosures of Chong and Yamazaki.

We reverse.

As evidence of obviousness of the claimed subject matter under section 103, the examiner relies on the combined disclosures of Chong and Yamazaki. Chong requires a capping layer to cover a metal layer on a particular semiconductor device before annealing it with a laser beam to activate source/drain regions and, at the same time, form a metal silicide layer. The presence of the capping layer, according to Chong, is important during laser beam annealing to form its particular semiconductor device. Thus, Chong not only does not teach the claimed exposed metal layer during annealing, but also does not teach the claimed heating temperature and time.

To remedy these deficiencies, the examiner relies on the disclosure of Yamazaki. Yamazaki teaches using laser beam annealing or non-laser beam heating annealing. When the non-laser beam annealing is employed, the claimed temperature may be used

Appeal No. 2003-2175
Application No. 09/712,234

without a capping layer (with an exposed metal layer). However, this non-laser beam heating technique requires two heating steps, one for activating source/drain regions and another for forming a metal silicide layer.

Thus, we determine that Chong and Yamazaki as a whole would have led one of ordinary skill in the art to anneal the claimed semiconductor device having an exposed metal layer with two non-laser beam heating steps or anneal the claimed semiconductor device having a capped (unexposed) metal layer with a single laser beam heating step. However, as correctly asserted by the appellant (Brief, page 9), “[t]here is no factual basis in Chong [and] Yamazaki to support the conclusion that one having ordinary skill in the art would have been led to anneal [the claimed] semiconductor device having an exposed metal layer with [the claimed] single heating step [(a temperature of about 350° C to less than 850° C for about 30 seconds to 60 minutes)] that activates source/drain regions and reacts the exposed metal layer with an underlying silicon layer [(forming a metal silicide layer) simultaneously]”. See *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002) (“This factual question of

Appeal No. 2003-2175
Application No. 09/712,234

motivation is material to patentability, and could not be resolved on subjective belief and unknown authority.”).

Accordingly, we are constrained to reverse the examiner’s decision rejecting all of the appealed claims under 35 U.S.C. § 103.

REVERSED

EDWARD C. KIMLIN)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
CHUNG K. PAK)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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LINDA R. POTEATE)	
Administrative Patent Judge)	

CKP/vsh

Appeal No. 2003-2175
Application No. 09/712,234

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