

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SESHADRI VIKRAM and WILLIAM J. SCHAEFER

Appeal No. 2004-0133
Application No. 09/668,031

ON BRIEF

Before KIMLIN, GARRIS and STAAB, Administrative Patent Judges.
KIMLIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1-3, 5, 7-9, 11 and 12, all of the claims remaining in the present application.

Claim 1 is illustrative:

1. A packaged integrated circuit comprising:

a die having first and second surfaces and a multiplicity of die contacts arranged on the first surface of the die;

a barrier layer deposited on the second surface of the die;

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a metallic layer deposited over the barrier layer to form a solderable surface over the second surface of the die;

a heat sink soldered to the metallic layer, wherein solder material used to couple the metallic layer to the heat sink provides good thermal conductivity between the die and the heat sink.

In the rejection of the appealed claims, the examiner relies on the following references:

Varteresian et al. (Varteresian)	4,499,659	Feb. 19, 1985
Lee	4,620,215	Oct. 28, 1986
Karnezos	5,843,808	Dec. 01, 1998

Appellants' claimed invention is directed to semiconductor packing arrangements and methods for forming such arrangements. The claimed packaged integrated circuit comprises a die having first and second surfaces with a multiplicity of die contacts on the first surface. The second surface is provided with a heat sink soldered to a metallic layer which, in turn is deposited over a barrier layer formed on the second surface. According to appellants' specification, the claimed manner of securing the heat sink to the second surface of the die is an improvement over the prior art use of an epoxy adhesive. We are told that "[t]he low thermal conductivity of the epoxy adhesive thus becomes a significant limitation of the overall effectiveness of the heat sink" (page 1 of specification, last sentence).

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Appealed claims 1, 5, 7 and 12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Lee. Claims 2, 3, 8, 9 and 11 stand rejected under 35 U.S.C. § 103 as being unpatentable over Lee in view of appellants' Admitted Prior Art (Figure 2), Karnezos and Varteresian.

Appellants submit at page 4 of the principal brief that with regard to the § 102 rejection, "claims 1, 5 and 7 will be argued as a group." Accordingly, claims 5 and 7 stand or fall together with claim 1.

We consider first the examiner's rejection of claims 1, 5, 7 and 12 under § 102 over Lee. We will sustain this rejection as it pertains to article claims 1, 5 and 7. As acknowledged by appellants, Figure 12 of Lee illustrates a die that has a gold-chromium alloy layer on its back surface. We find that this alloy layer meets the requirement of the claimed barrier layer deposited on the second surface of the die. Also, the heat sink 80 of Figure 12 is joined to the back surface of the die through a gold layer, which corresponds to appellants' claimed metallic layer. In its final form, the chip of Figure 12 comprises a heat sink soldered to the back surface of a die wherein a barrier layer is deposited on the second surface, and a metallic gold

layer is deposited over the barrier layer. It is of no moment that Lee's method of attaching the heat sink to the second surface of the die is somewhat different to appellants' method inasmuch as claims 1, 5, and 7 define a product.

The § 102 rejection of claim 12 is another matter. Claim 12 provides a method wherein the die is provided having a barrier layer and a metallic layer deposited on its back surface, and such solderable back surface is then soldered to a metallic heat sink. This methodology is not described in the embodiments corresponding to Figures 11 and 12 of Lee which provide only a gold-chromium alloy on the back surface of the die before it is soldered to a heat sink. While the examiner relies on Figures 3 and 7 of Lee, we agree with appellants that the reference makes it clear that Figure 7 is directed to providing a heat sink on the front, not back surface of the die. Lee discloses at column 6, lines 56 et seq that Figure 7 is directed to providing heat sink 75 on the front surface of the die. Also, at column 7, lines 10 et seq, the reference explicitly discloses that Figures 11 and 12 illustrate two alternative methods of binding heat sink 80 to the back surface of the die.¹ Although the examiner

¹ Although Lee describes "top surface 71", inactive surface 71 of Lee corresponds to appellants' second back surface.

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maintains that appellants fail "to appreciate the flexibility taught by the invention of Lee et al that is shown in the various embodiments" (page 7 of answer, last paragraph), the examiner has pointed to no disclosure in Lee which supports the position that the means for bonding a heat sink to the back surface can be the same as the means for bonding a heat sink to the first surface. On the other hand, we find Lee to be quite specific in teaching that Figure 6 applies to the heat sink on the first surface whereas Figures 11 and 12 apply to the heat sink on the back surface. Accordingly, we will not sustain the examiner's § 102 rejection of claim 12.

We will sustain the examiner's rejection of claims 2, 3, 8 and 9 under § 103. Claim 2 requires an array of I/O pads on the first surface of a substrate and an array of contacts on the second surface of the substrate, wherein the die of claim 1 is mounted such that the die contacts are coupled to adjacent I/O pads. Appellants acknowledge at page 10 of the principal brief that "the attachment of integrated circuits to substrates having I/O pads is generally well known in the packaging arts" and that "flip-chip mounting of integrated circuits onto substrates having I/O pads is generally known" (page 10 of principal brief, first paragraph). It is appellants' contention that "the claimed

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combination wherein a die is **flip-chip mounted** to a substrate and a heat sink is soldered to the metalized back surface of the die is a unique combination that is in no way suggested by any reasonable combination of the art of record" (id.). We disagree. Our finding of obviousness logically follows from our finding that the packaged integrated circuit of claim 1 is described by Lee and appellants' acknowledgment that flip-chip mounting of integrated circuits having I/O pads was known at the time of the filing of the present application. As noted by the examiner, the thrust of the invention disclosed in appellants' specification is replacing the prior art epoxy adhesive with the claimed barrier and metallic layers for bonding a heat sink to the back surface of the die. Our same rationale applies to claim 8 insofar as appellants have not presented a substantive argument specific to claim 8, but submit that "claim 8 is patentable over the art of record for all the reasons set forth above with respect to claims 1 and 2" (page 11 of principal brief, second paragraph).

Concerning claim 9, which defines a semiconductor wafer comprising a plurality of dice with the metallic and barrier layers deposited on the second surface of the wafer, we agree with the examiner that it would have been obvious for one of

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ordinary skill in the art to apply the disclosure associated with Lee's Figure 12 to a wafer as well as a single die. Since a wafer is diced to produce singular dies, one of ordinary skill in the art would have been faced with the option of providing the heat sink to the back surface of the die either individually, after dicing the wafer, or to the entire wafer before dicing. In our view, one of ordinary skill in the art would have found it obvious and expedient to provide the heat sink and intermediate layers to the back surface of the wafer before it is diced into individual dies rather than processing each single die individually.

Regarding the method of claim 11 which comprises depositing the barrier and metallic layers on the back surface of the wafer before dicing to provide individual die, and soldering a metallic heat sink to the back surface of selected die, we find, as explained above, that it would have been obvious for one of ordinary skill in the art to provide the chrome alloy layer 72A, gold 84 and heat sink 80 to the back surface of the wafer before dicing as well as to individual die after dicing. However, as also explained above, with respect to the examiner's § 102 rejection of method claim 12, Lee does not describe the steps of

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claim 11, and the examiner has not established that it would have been obvious for one of ordinary skill in the art to modify the steps according to Lee's Figure 12 to achieve the steps recited in claim 11. Accordingly, we are constrained to reverse the examiner's § 103 rejection of claim 11.

One final point remains. Upon return of this application, the examiner should explore the obviousness of modifying the method steps in accordance with Lee's Figure 12 such that the gold layer is deposited upon the chromium alloy before the heat sink is soldered to the back surface of chip 70. While we note appellants' statement at page 1 of the reply brief that "in semiconductor processing and packaging, front side processing is typically quite different from back side processing" (last paragraph), such distinctions have not been fully developed on this record.

In conclusion, based on the foregoing, the examiner's § 102 rejection of claims 1, 5 and 7 is affirmed whereas the § 102 rejection of claim 12 is reversed. Also, the examiner's § 103 rejection of claims 2, 3, 8 and 9 is affirmed while the § 103 rejection of claim 11 is reversed. As a result, the examiner's decision rejecting the appealed claims is affirmed-in-part.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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Administrative Patent Judge)	
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BRADLEY R. GARRIS)	APPEALS AND
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LAWRENCE J. STAAB)	
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