

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 40

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AARON SCHOENFELD
and RAJESH SOMASEKHARAN

Appeal No. 2004-0393
Application 09/388,824¹

HEARD: May 6, 2004

Before BARRETT, RUGGIERO, and LEVY, Administrative Patent Judges.
BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed September 1, 1999, entitled "Integrated Circuit Having Conductive Paths of Different Heights Formed from the Same Layer Structure and Method for Forming the Same," which is a division of Application 08/928,556, filed September 12, 1997, now abandoned.

Appeal No. 2004-0393
Application 09/388,824

This is a decision on appeal under 35 U.S.C. § 134(a) from the final rejection of claims 53-60.

We affirm-in-part.

BACKGROUND

The invention relates to a method of forming an integrated circuit having conductive paths of different heights.

Claim 53 is reproduced below.

53. A method for forming a memory circuit, comprising:

forming a structure on a substrate, the structure including a first conductive layer disposed on the substrate and a second conductive layer disposed on the first conductive layer;

removing the second conductive layer from a first region of the structure while preserving the second conductive layer in a second region of the structure;

forming digit lines from the first conductive layer in the first region of the substrate in a direction normal to the substrate; and

forming a high current line in a spaced parallel relationship with the digit lines, the high current line being formed from the first and second conductive layers in the second region of the substrate.

The examiner relies on the following reference:

Jimenez

5,543,358

August 6, 1996

Appeal No. 2004-0393
Application 09/388,824

Claims 53-60 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Jimenez.

OPINION

Claims 53, 54, 57, and 58

Claims 53, 54, 57, and 58 stand or fall together with independent claim 53.

Initially, we must determine what weight, if any, to give to the phrase "for forming a memory circuit" and the term "digit lines." Claim 53 is a method claim "for forming a memory circuit." No memory circuit is recited in the claim body and, thus, "for forming a memory circuit" is considered a statement of intended use. The examiner previously stated that "digit lines" was "a label or statement of intended use" (FR3). We agree. The term "digit lines" refers to conductive lines that serve the function of bit lines of a memory circuit; however, no memory circuit is claimed. Thus, we interpret "digit lines" to be like a statement of intended use or function, which only requires that the structure be capable of performing that use. Appellants have not shown why metal lines M1-1 and M1-2 are not capable of performing the function. Looked at in another way, appellants have not shown that the product produced by the method of

Appeal No. 2004-0393
Application 09/388,824

claim 53 is different than the product in Jimenez, except in the way the conductive lines are intended to be used.

The examiner has unnecessarily made the rejection more difficult by relying on 35 U.S.C. § 102 instead of § 103. Jimenez discloses that the invention relates to fabrication of so-called "Smart Power" components that include power elements and a control logic portion on the same chip (col. 1, lines 7-11). Thus, Jimenez does not teach that the control logic portions are used for "digit lines." Jimenez discloses different thickness metallizations for power and logic circuits used together (col. 1, lines 13-26). In view of this teaching, it would have been obvious to one of ordinary skill to apply Jimenez to a memory device having both power and logic memory portions on the same chip, where the logic memory portion necessarily includes digit lines. The examiner's finding of "formation of digit lines to be inherent in the disclosure of Jimenez" (answer, p. 5) is erroneous because Jimenez does not disclose that the logic portion of the "Smart Power" component necessarily has a memory. The examiner's reference to Segawa in support of the inherency rejection is not appropriate for an anticipation rejection and, in any case, Segawa does not tend to prove that

Appeal No. 2004-0393
Application 09/388,824

digit lines are inherent in Jimenez. Nevertheless, we sustain the rejection based on claim interpretation.

Appellants argue that metal layer 7 is not "disposed on" the metal layer 2 in Jimenez because there is an etch mask layer 11-1 and 11-2 on the portion of the metal layer 2 used to form the thinner lines (reply brief, p. 2). This is a new argument presented for the first time in the reply brief. Since the examiner has no right to file a supplemental examiner's answer in response to a reply brief, we have no response by the examiner.

In the semiconductor art, "disposed on," and similar limitations, such as "on top of," "deposited on," etc., are commonly interpreted to not exclude intermediate layers, e.g., a piece of paper may be "disposed on" a desk even though it sits on top of other pieces of paper. Appellants have not claimed "disposed directly on," which would distinguish over Jimenez.

For the reasons stated above, we sustain the rejection of claims 53, 54, 57, and 58.

Claims 55, 56, 59, and 60

Claims 56, 56, 59, and 60 stand or fall together with independent claim 55.

The examiner finds that Jimenez discloses forming a first conductive layer that "comprises a first part of layer 2 (Figure 2A, and Column 3, lines 25-26)" (answer, p. 3) and forming a second conductive layer that "comprises a second part of layer 2 (Figure 2C, and Column 3, lines 37-40)" (answer, p. 4). That is, the examiner finds that forming a single layer in Jimenez anticipates forming first and second layers, as recited in claim 55.

Appellants argue that Jimenez does not teach that the first metal layer 2 can be formed by first and second parts of the layer 2 (brief, p. 7).

We agree with appellants that a single layer in Jimenez cannot reasonably be interpreted to meet the limitation of forming discrete first and second conductive layers as called for in claim 55. The rejection of claims 55, 56, 59, and 60 is reversed.

CONCLUSION

The rejection of claims 53, 54, 57, and 58 is sustained.

The rejection of claims 55, 56, 59, and 60 is reversed.

Appeal No. 2004-0393
Application 09/388,824

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

LEE E. BARRETT)	
Administrative Patent Judge)	
)	
)	
)	
)	BOARD OF PATENT
JOSEPH F. RUGGIERO)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
STUART S. LEVY)	
Administrative Patent Judge)	

Appeal No. 2004-0393
Application 09/388,824

DORSEY & WHITNEY LLP
INTELLECTUAL PROPERTY DEPARTMENT
SUITE 3400
1420 FIFTH AVENUE
SEATTLE, WA 98101