

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 35

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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***Ex parte*** RAYMOND S. TETRICK

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Appeal No. 2004-0442  
Application No. 09/222,953

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ON BRIEF<sup>1</sup>

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Before HAIRSTON, GROSS, and BLANKENSHIP, ***Administrative Patent Judges.***

GROSS, ***Administrative Patent Judge.***

***DECISION ON APPEAL***

This is a decision on appeal from the examiner's final rejection of claims 1 through 21, which are all of the claims pending in this application.

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<sup>1</sup> We note that the hearing scheduled for May 18, 2004 was waived by appellant.

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Appellant's invention relates to an averaging measurement circuit using a subtracter, an adder, and a single register. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. An averaging measurement circuit comprising:

a register adapted to successively store a series of data words having a plurality of bits, said register adapted to provide, for each of said data words, a first output signal comprising all of the plurality of bits of the data word and a second output signal comprising a number of the higher order bits of the data word;

a subtracter adapted to subtract each second output signal of said register from a corresponding data sample and output a corresponding subtraction result; and

an adder to add each first output signal of the register to a corresponding subtraction result and store the result in said register.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Ito	4,829,460	May 09, 1989
Ono et al. (Ono)	5,448,508	Sep. 05, 1995

Claims 1, 4, 6, 9, 11, 17, and 20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ono.

Claims 5, 10, 16, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ono.

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Claims 2, 3, 7, 8, 12 through 15, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ono in view of Ito.

Reference is made to the Examiner's Answer (Paper No. 23, mailed March 19, 2003) for the examiner's complete reasoning in support of the rejections, and to appellant's Brief (Paper No. 22, filed January 8, 2003) and Reply Brief (Paper No. 24, filed May 19, 2003) for appellant's arguments thereagainst.

#### **OPINION**

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellant and the examiner. As a consequence of our review, we will reverse the anticipation rejection of claims 1, 4, 6, 9, 11, 17, and 20 and also the obviousness rejections of claims 2, 3, 5, 7, 8, 10, 12 through 16, 18, 19, and 21.

Each of independent claims 1, 6, 11, and 17 recites, in pertinent part, a register. The examiner (Answer, page 4) points to element 25 in Ono's Figure 6A as satisfying the claimed register. However, Ono discloses (column 3, lines 31-32) that element 25 is a latch circuit. The examiner, recognizing that Ono does not explicitly disclose a register, asserts (Answer,

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page 6) that "'register' and 'latch' are alternative terms or labels for referring [sic, to] a storage device." Appellant argues (Brief, page 7) that the examiner has failed to establish anticipation since the examiner has admitted that Ono discloses an alternative to the claimed register rather than the register itself. We agree.

"It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim." *In re King*, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986). *See also Lindemann Maschinenfabrik GMBH v. American Hoist and Derrick*, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). Claims 1, 6, 11, and 17 all require a register. Ono discloses a latch circuit, not a register. Although registers and latches are both types of storage and both may be comprised of flip flops, they are not the same. A register is a high-speed memory location in a computer's CPU used to store digits, whereas a latch is a digital logic circuit having a data input, a clock input, and an output and is used to store a state. Therefore, the disclosure of a latch does not anticipate the claimed register. Accordingly, we cannot sustain the anticipation rejection of claims 1, 6, 11, and 17 and their dependents, claims 4, 9, and 20.

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Appellant further argues (Brief, page 8), regarding claim 6, that Ono fails to disclose a processor as claimed. Specifically, appellant contends (Brief, pages 8-9) that Ono discloses a PSK demodulator rather than a processor and that Ono "does not measure the moving average of a value relating to the operation of the demodulator." We disagree. Ono discloses (column 1, lines 7-10) that the invention "relates to a circuit for computing a moving average value of data in digital signal processing." Thus, Ono discloses calculating a moving average of a value in a digital signal processor. Nonetheless, as indicated *supra*, Ono fails to disclose the claimed register, and therefore fails to anticipate claim 6.

Regarding claims 4, 9, and 20, appellant argues (Brief, page 9) that Ono fails to meet the claimed limitation that the first output signal has the same number of bits as the data sample. The examiner responds (Answer, page 7) that Ono "clearly shows in figure 3 the moving average signal (D0) having the same number of bit of data sample (8 bits)." The first output signal, however, as recited in claims 1, 6, and 17 from which claims 4, 9, and 20 depend, respectively, is what is added to the subtraction result. In Ono (column 5, lines 6-15) the subtraction data  $D_1$  is added by an adder to accumulation data  $D_3$ .

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Ono indicates (column 5, lines 34-35) that  $D_3$  has 15 bits, whereas, the data sample,  $D_i$ , has 8 bits (see column 5, lines 9-10). Therefore, Ono fails to anticipate claims 4, 9, and 20 for the additional reason that Ono's first output signal does not have the same number of bits as the data sample.

As to the obviousness rejection of claims 5, 10, 16, and 21, the examiner has presented no evidence to overcome the deficiencies in the rejection of the base claims. Further, each of the aforementioned claims recites that the register, subtracter, and adder are all "included in the silicon of a chip." The examiner (Answer, page 5) recognizes that Ono does not disclose a silicon chip, but asserts that "the implementation of a processing circuit in a silicon ship [sic, chip] is so well-known in the art . . . , a person of ordinary skill in the art would have found it obvious to do so in order to reduce cost and circuitry area." Appellant (Brief, page 10) argues that the examiner has failed to point to any teaching or suggestion in the prior art for the proposed modification. A factual inquiry whether to modify a reference must be based on objective evidence of record, not merely conclusionary statements of the examiner. **See In re Lee**, 277 F.2d 1338, 1342-43, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002). As the examiner has failed to supply any objective

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evidence of obviousness, we cannot sustain the obviousness rejection of claims 5, 10, 16, and 21.

Regarding the obviousness rejection of claims 2, 3, 7, 8, 12 through 15, 18, and 19, Ito does not overcome the shortcomings of Ono for the limitations of the independent claims. Further, as pointed out by appellant (Brief, page 12) the examiner has not pointed to any teaching or suggestion in Ito for modifying Ono to include multiplexors. Although Ito may disclose multiplexors, there must be some suggestion in the prior art to motivate the skilled artisan to use Ito's multiplexors in Ono's device, and the examiner has pointed to no such teaching or suggestion. Accordingly, we cannot sustain the obviousness rejection of claims 2, 3, 7, 8, 12 through 15, 18, and 19.

#### **CONCLUSION**

The decision of the examiner rejecting claims 1, 4, 6, 9, 11, 17, and 20 under 35 U.S.C. § 102(b) is reversed. The

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decision of the examiner rejecting claims 2, 3, 5, 7, 8, 10, 12  
through 16, 18, 19, and 21 under 35 U.S.C. § 103 is reversed.

**REVERSED**

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
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	)	BOARD OF PATENT
ANITA PELLMAN GROSS	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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	)	
HOWARD B. BLANKENSHIP	)	
Administrative Patent Judge	)	

APG:clm

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