

The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte FONG PONG, LANCE RUSSELL and TUNG NGUYEN

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Appeal No. 2004-0538  
Application No. 09/976,495

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ON BRIEF

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Before KRASS, SAADAT and NAPPI, Administrative **Patent Judges**.

NAPPI, **Administrative Patent Judge**.

**DECISION ON APPEAL**

This is a decision on appeal under 35 U.S.C. § 134 of the final rejection of claims 1 through 6, which constitute all the claims in the application.

**Invention**

The invention relates to a multi-processor computer system, which includes a distributed shared memory, see page 3 of appellants' specification. The system includes a cache flushing engine which forces the local cache to write data back to

memory, see page 5 of appellants' specification.  
Claim 1 is representative of the invention and reproduced below:

1. A multi-processor computer system comprising:  
a plurality of processors;  
  
a plurality of caches, each of said plurality of caches operatively connected to one of said plurality of processors;  
  
a first system control unit operatively associated with one of said plurality of processors and operatively connected to one of said plurality of caches, said system control unit having a cache flushing engine operatively connected to said one of said plurality of caches;  
  
a second system control unit operatively associated with said first system control unit and operatively connected to said cache flushing engine;  
  
a memory operatively connected to said second system control unit; and  
  
said first system control unit responsive to an update of said one of said plurality of caches operatively connected therewith to flush said update to said second system control unit and assure said update is entered into said memory.

### References

The references relied upon by the examiner are:

Appellants admitted prior art (AAPA) on pages 1-3 of the originally filed specification.

James et al. (James)	5,961,623	Oct 5, 1999 (filed Aug. 29, 1996)
Hagersten	5,892,970	April 6, 1999 (filed July 1, 1996)

### **Rejection at Issue**

Claim 1 stands rejected under 35 U.S.C. § 102 as being anticipated by AAPA. Claims 2 through 6 stand rejected under 35 U.S.C. § 103 as being obvious over AAPA in view of either Hagersten or James. Throughout the opinion we make reference to the Briefs<sup>1</sup> and the answer for the respective details thereof.

### **Opinion**

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation and obviousness relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

With full consideration being given to the subject matter on appeal, the examiner's rejection and the arguments of appellants and examiner, for the reasons stated *infra* we will not sustain the examiner's rejection of claim 1 under 35 U.S.C. § 102, nor will we sustain the examiner's rejection of claims 2 through 6 under 35 U.S.C. § 103.

Appellants assert, on page 3 of the brief, that the AAPA teaches a coherence mechanism which provides for a write-back of data to memories when there is new data in the cache. On page 4, of the brief, appellants argue that the coherence controller is not the same as the claimed cache flushing engine. Appellants argue:

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<sup>1</sup>Appellants filed an Appeal Brief on June 4, 2003 and appellants filed a Reply Brief on August 18, 2003.

AAPA allows the new value to be seen and entered into the home memory or, more importantly, only partially or erroneously entered in the event of a failure of the sending node before the entire new value is in the home memory. The coherence controller does not “flush”, or force, the new value into the second system control unit so as to “assure” the new value is actually entered into the home memory.

In response to these arguments, the examiner asserts, on page 5 of the answer, the AAPA “clearly states that the prior art writes back (i.e., flushes) the data to the other nodes.” Further, the examiner notes that in the AAPA “The home node employs a coherence protocol to ensure that when a node writes a new value to the memory block, all other nodes see this latest value.” (Page 6 of the examiner’s answer, quoting page 2 of appellants’ specification). Finally, the examiner concludes “Appellants can not distinguish their invention which ‘flushes’ and ‘assures,’ from the prior art, which merely *writes-back all updates, that ensures that all other nodes see the updated value* and that further *guarantees coherency.*” (emphasis original).

We disagree with the examiner’s interpretation of the claim and his conclusion that the claimed invention is not differentiated from AAPA. Claims will be given their broadest reasonable interpretation consistent with the specification, limitations appearing in the specification will not be read into the claims. *In re Etter* 756 F.2d 852, 858, 225 USPQ 1, 5 (Fed. Cir. 1985). In analyzing the scope of the claim, office personnel must rely on the appellant’s disclosure to properly determine the meaning of the terms used in the claims. *Markman v. Westview Instruments, Inc.*, 52 F3d 967, 980, 34 USPQ2d 1321, 1330 (Fed. Cir. 1995). “[I]nterpreting what is *meant* by a word in a claim ‘is not to be confused with adding an extraneous limitation appearing in the specification, which is improper.’”

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(emphasis original) *In re Cruciferous Sprout Litigation*, 301 F.3d 1343, 1348, 64 USPQ2d 1202, 1205, (Fed. Cir. 2002) (citing *Intervet America Inc v. Kee-Vet Laboratories Inc.* 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)). “[T]he terms used in the claims bear a “heavy presumption” that they mean what they say and have the ordinary meaning that would be attributed to those words by persons skilled in the relevant art.” *Texas Digital Sys, Inc. v. Telegenix, Inc.*, 308 F.3d 1193, 1202, 64 USPQ2d 1812, 1817 (Fed. Cir. 2002). “Moreover, the intrinsic record also must be examined in every case to determine whether the presumption of ordinary and customary meaning is rebutted.” (citation omitted). “Indeed, the intrinsic record may show that the specification uses the words in a manner clearly inconsistent with the ordinary meaning reflected, for example, in a dictionary definition. In such a case, the inconsistent dictionary definition must be rejected.” *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d at 1204, 64 USPQ2d at 1819 (Fed. Cir. 2002). (“[A] common meaning, such as one expressed in a relevant dictionary, that flies in the face of the patent disclosure is undeserving of fealty.”); *Id.* (citing *Liebscher v. Boothroyd*, 258 F.2d 948, 951, 119 USPQ 133, 135 (C.C.P.A. 1958) (“Indiscriminate reliance on definitions found in dictionaries can often produce absurd results.”)). “In short, the presumption in favor of a dictionary definition will be overcome where the patentee, acting as his or her own lexicographer, has clearly set forth an explicit definition of the term different from its ordinary meaning.” *Id.* “Further, the presumption also will be rebutted if the inventor has disavowed or disclaimed scope of coverage, by using words or expressions of manifest exclusion or restriction, representing

a clear disavowal of claim scope.” *Id.*

Claim 1 contains the limitations of “a cache flushing engine” and “said first system control unit responsive to an update of said one of said plurality of caches operatively connected therewith to flush said update to said second system control unit and assure said update is entered into said memory.” The flush command is discussed on page 5 of the appellants’ specification as a command that will “force, or ‘flush’, the local cache 205 to write back the new values for locations... to the temporary buffer 315 in the home node.” This explanation is constant with the dictionary definition of flush “to clear the contents of a buffer, saving changed data in disk.”<sup>2</sup> The definition also seems to be consistent with the meaning used in the prior art, for example column 22, lines 23 to 26 of Hagersten, states “Flush requests cause copies of the coherency unit to be invalidated. Modified copies are returned to the home node.” Thus, we consider the scope of claim 1 to include a flush engine which forces a write of data from the cache associated with a first control unit to memory associated with a second control unit.

We find that the AAPA teaches a multiprocessor system where data is kept by a home node in a home memory and the other nodes may contain copies of the data. The home node maintains a directory of nodes that have copies. If a node does not have a copy it requests it from the home node. See page 1 of appellants’ specification. If the home node does not have the most up to date copy (stale copy) the home node directs the requesting node to the node that does have an up to date copy. See appellants’ specification page 2. The AAPA states, “the home node employs a coherence protocol to

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<sup>2</sup> Definition from Microsoft Press, Computer Dictionary, 1994.

ensure that when a node writes a new value to the memory block, all other nodes see this latest value.” We do not find that the coherence protocol functions to “flush” the cache as is claimed, as this section of the AAPA is discussing the case where a node is writing data to it’s own memory block and not the memory block of another node. Thus, we do not find that the AAPA teaches a first system control unit, with a cache flushing engine, where the first control unit is responsive to an update of one of said plurality of caches operatively connected therewith to flush said update to a second system control unit and assure said update is entered into said memory, as is claimed. Accordingly, we will not sustain the examiner’s rejection of claim 1.

We next turn to the rejection of claims 2 through 6 under 35 U.S.C. § 103. Claims 2 through 6 are dependent upon claim 1, and as such necessarily include the same limitations as claim 1. The examiner has not asserted that either Hagersten or James teaches or suggests cache flushing, but rather the examiner relies upon Hagersten and James to teach the limitations directed to buffers. See pages 3 and 5 of the Examiner’ Answer. We do not find that James teaches flushing. As addressed *supra*, we do find that Hagersten addresses the function of flushing. However, we do not find that Hagersten teaches the interrelationship between the first and second control units and the flushing engine as is claimed. Accordingly, we will not sustain the rejection of claims 2 through 6.

#### **Other issues**

Though, the issues is not before us, we note that dependent claim 4 introduces the limitation “a temporary buffer connected through said second system control unit to said

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memory...” we find this limitation to be ambiguous as it does not identify if the antecedent memory is the memory associated with the first of second system control unit. The examiner and applicant should take appropriate action to eliminate this ambiguity in claim 4.

For the forgoing reasons, we reverse the examiner’s rejection of Claim 1 under 35 U.S.C. § 102 as being anticipated by AAPA and the examiner’s rejection of Claims 2 through 7 under 35 U.S.C. § 103 as being obvious over AAPA in view of either Hagersten or James.

**REVERSED**

ERROL A. KRASS	)	
Administrative Patent Judge	)	
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	)	
	)	
MAHSHID D. SAADAT	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
	)	INTERFERENCES
	)	
	)	
ROBERT NAPPI	)	
Administrative Patent Judge	)	

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