The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

Paper 32

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HONGJIANG SONG

Appeal No. 2004-0593
Application No. 09/606,688

ON BRIEF

Before LEE, MEDLEY, and MOORE, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge.*

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the final rejection of claims 1-4, 7-10, 13-16, 25, 27, 31, 35, and 39. Claims 5, 6, 11, 12, 17, 18, 28, 29, 32, 33, 36, and 37 are allowable; while claims 19-24, 26, 30, 34, and 38 are allowable if rewritten. Accordingly, claims 1-4, 7-10, 13-16, 25, 27, 31, 35, and 39 are before us on this appeal.

REPRESENTATIVE CLAIMS

The appellant has not expressly grouped the claims in any groups, although claims 1, 7, 13, and 25 appear to be argued in one group (Appeal Brief, page 5, lines 21-23), claims 3, 9, and 15

in another group (Appeal Brief, page 7, lines 15-18), claims 4, 10, and 16 as a third group (Appeal Brief, page 7, lines 19-21), while claims 27, 31, 35, and 39 appear to be argued in yet another group. (Appeal Brief, page 9, lines 6-8). Accordingly, we select claims 1, 3, 4, and 27 as representative of the claims on appeal. Note In re Dance, 160 F.3d 1339, 1340 n.2, 48 USPQ2d 1635, 1636 n.2 (Fed. Cir. 1998); In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

These claims read as follows:

1. A buffer/voltage-mirror arrangement comprising:
a plurality of stages, each comprising:
electrically parallel branches of a first transistor connected in series with a second transistor, and a third transistor connected in series with a fourth transistor, said second and fourth transistors being of an inverse type to that of said first and third transistors, where said first and third transistors are substantially matched and said second and fourth transistors are substantially matched, a gate interconnection electrically connecting gates of said first and second transistors to one another, and an intermediate electrical connection directly connecting all of the gates of said third and fourth transistors, an intermediate point between said first and second transistors and an intermediate point between said third and fourth transistors to one another;

wherein said gate interconnection of a first stage represents an input, wherein said intermediate electrical connection of a preceding stage is electrically connected to said gate interconnection of a succeeding stage, and said intermediate electrical connection of a final stage represents an output, and wherein said buffer/voltage-mirror arrangement is adapted to cause an output voltage on said output to mirror an input voltage on said input by a predetermined factor.

3. A buffer/voltage-mirror arrangement as claimed in claim 1, wherein ones of said first, second, third and fourth transistors of an input stage of said buffer/voltage-mirror arrangement are smaller in size than other ones of said first, second, third and fourth transistors of other stages so as to minimize an influence of said buffer/voltage-mirror arrangement on any input circuit to which said buffer/voltage-mirror arrangement is attached.

4. A buffer/voltage-mirror arrangement as claimed in claim 1, wherein ones of said first, second, third and fourth transistors of an output stage of said buffer/voltage-mirror arrangement are larger in size than other ones of said first, second, third and fourth transistors of other stages so as to increase a driving capacity of said buffer/voltage-mirror arrangement.

27. A buffer/voltage-mirror arrangement as claimed in claim 1, wherein said a plurality of stages are arranged in a non-feedback, series cascade of stages.

The Reference

In rejecting the claims under 35 U.S.C. §102(b), the examiner relies upon the following reference:

Rempfer et al. (Rempfer) 5,070,259 Dec. 03, 1991

The Rejection

Claims 1-4, 7-10, 13-16, 25, 27, 31, 35, and 39 stand rejected under 35 U.S.C. §102(b) as being anticipated by Rempfer.

The Invention

The invention relates to a buffer/voltage-mirror circuit for use in, e.g., automated test equipment. (Specification, page 1, lines 2-3 and 14). The circuit is designed to provide

nonintrusive observability of very sensitive internal nodes in mixed-signal integrated circuits (Id., page 5, lines 4-5). Further details of the claimed invention are found in the claims reproduced above.

The Rejection of Claims 1-4, 7-10, 13-16, 25, 27, 31, 35, and 39 Under 35 U.S.C. § 102(b)

The examiner has found that Rempfer discloses a multi-stage circuit wherein each stage has electrically parallel branches of a first transistor connected in series with a second transistor, and a third transistor connected in series with a fourth transistor. The second and fourth transistors are of an inverse type to that of the first and third transistors (NMOS and PMOS transistors, respectively). (Examiner's Answer, page 3, line 19 - page 4, line 3).

The examiner has also found that the transistors are matched, as in an integrated circuit the transistors are considered to be matched unless otherwise stated. (Id., page 4, lines 4-6).

The examiner has finally found that Rempfer describes a gate interconnection electrically connecting gates of a first and second transistor to one another and an intermediate electrical connection directly connecting all of the gates of the third and fourth transistors, an intermediate point between the first and

second transistors, and an intermediate point between the third and fourth transistors to each other. (Id, page 4, lines 10-14).

Finally, the examiner has found that the input of the first stage represents an input, and the intermediate electrical connection of a preceding stage is electrically connected to the gate interconnection of a succeeding stage, and the intermediate electrical connection of a final stage represents an output. The recitation relating to the mirroring of output voltage is said to be met by the reference as the structure of the claim is fully met. (Id., page 4, lines 14-20).

The appellant first urges that Rempfer does not use the term “matched” or “substantially matched” in reference to the transistors. (Appeal Brief, page 5, lines 21-24). As a consequence, it is reasoned, the rejected claims are not anticipated by Rempfer.

In examining a patent claim, the PTO must apply the broadest reasonable meaning to the claim language, taking into account any definitions presented in the specification. In re Yamamoto, 740 F.2d 1569, 1571, 222 USPQ 934, 936 (Fed. Cir. 1984). Words in a claim are to be given their ordinary and accustomed meaning, unless the inventor chose to be his own lexicographer in the specification. Lantech, Inc. v. Keip Mach. Co., 32 F.3d 542, 547,

31 USPQ2d 1666, 1670 (Fed. Cir. 1994).

The appellant urges that the examiner improperly equated transistor type with "matching," which is stated by the appellant to mean specifically electrically and/or constructively balanced to one another, as opposed to randomly picked. (Appeal Brief, page 6, lines 7-15). The appellant further urges that:

> 'Matched' has a very well known and established meaning in the electronic art, i.e., it means that the two transistors are specifically electrically and/or constructively balanced to one another. Beyond established meaning, Appellant's prior prosecution arguments further made it clear that "matched" means transistors electrically and/or constructively balanced to one another. It takes special care and testing to achieve matched transistors, even in the integrated circuit art. That is, even transistors processed together on a same IC most likely will not be matched, as it is well known that processing variations exist even at short distances across an IC. Because matched transistors are hard to achieve, they are more expensive and thus are sold specially and used sparingly in the art. They are the exception rather than the rule. The Examiner's Answer comment that "it is considered in the art that the transistors in an integrated circuit are "matched transistors" unless otherwise specifically stated in the reference" does not seem to have any basis in the art and does not appreciate the difficulty/special-care needed to achieve matched transistors. Such comments seem to take an opposite stance, *i.e.*, that all IC transistors are automatically matched. Anyone skilled in the art, and even engineering students, know that this is not the case. There are thousands of patents directed to methods, constructions, etc. for achieving matched transistors. (Reply Brief, page 2, line 28-page 3, line 16).

This passage asserts many facts and conclusions; however, it is devoid of a single reference, treatise, dictionary, or declaration

in support thereof. We decline to search the "thousands" of patents to support the appellant's contention that this knowledge is within the purview of even electrical engineering students. It is well settled that mere lawyer's arguments and conclusory statements, which are unsupported by factual evidence, are entitled to little probative value. In re Geisler, 116 F.3d 1465, 1470, 43 USPQ2d 1362, 1365 (Fed. Cir. 1997); In re De Blauwe, 736 F.2d 699, 705, 222 USPQ 191, 196 (Fed. Cir. 1984); In re Wood, 582 F.2d 638, 642, 199 USPQ 137, 140 (CCPA 1978); In re Lindner, 457 F.2d 506, 508-09, 173 USPQ 356, 358 (CCPA 1972). We are unpersuaded by the appellant's argument.

We instead first look to the specification for any definition of "matched" which the appellant may have used. The only disclosure we have found is in the paragraph spanning pages 8 and 9, which reads as follows:

> An advantage of the Fig. 2 example buffer/voltage-mirror circuit is that it is very easy to design and implement in a semiconductor IC, and such does not require excessive semiconductor real estate. Further, if the circuit is laid out on the semiconductor die such that the transistor devices are geographically close to one another, than all such transistors will be subjected to substantially the same semiconductor processing and local environment leading to the advantage that the various transistor devices can be easily matched to one another. Practice of the present invention may also be made with discreet (as opposed to semiconductor) circuits. However, such would require matching of components, with any degree of mismatching affecting an

accuracy of the buffer/voltage-mirror circuit.[1]

1 We note that it is unclear if there is sufficient language in the specification supporting the April 5, 2002 amendment of the claims limiting the first and third transistors, and second and fourth transistors, respectively, to being "matched or substantially matched." This issue should be addressed in the event of further prosecution.

No further discussion of what is “matched” or “substantially matched” appears in the specification, to our knowledge. Indeed, this passage from the specification appears to undercut the appellant’s argument that IC device transistors are not ordinarily “matched” within the broadest reasonable interpretation of the word.

Similar to the position taken by the examiner, it would appear that the appellant’s own specification indicates that transistors on the same integrated circuit are generally matched (as opposed to discrete components), unless otherwise stated. Rempfer’s transistors appear to be manufactured on the same IC. Consequently, we agree with the examiner that Rempfer’s transistors are properly found to be “matched” or “substantially matched.” The appellant has provided no convincing evidence to the contrary.

The appellant next urges that claims 1, 7, 13, and 25 recite a buffer/voltage-mirror arrangement adapted to cause an output voltage on said output to mirror an input voltage on said input by a predetermined factor. Rempfer, it is said, discloses an amplifier configuration wherein the W/L ratio of the first and second transistors is N times larger than the W/L ratio of the third and fourth transistors. (Appeal Brief, page 6, line 27-page

7, line 9).

The claimed subject matter does not exclude the amplification effect of Rempfer; indeed, the claims expressly include it as a possibility by acknowledging that the mirroring factor may be present. Furthermore, a review of Rempfer figure 4 reveals the same circuitry as claimed by the appellant. We find no error in the examiner's conclusion that it functions as claimed. Again, the appellant has provided no convincing evidence otherwise. Accordingly, we are unpersuaded by this argument.

Next, the appellant urges that dependent claims 3, 9, and 15 recite that ones of the first, second, third, and fourth transistors of an input stage are smaller than other ones of first, second, third, and fourth transistors of other stages. Claims 4, 10, and 16 provide the reverse, that the input stage transistors are larger. (Appeal Brief, page 7, lines 15-25).

Rempfer, it is urged, does not meet the claimed limitations in that it only discloses differences between transistors within the one stage. (Appeal Brief, page 8).

However, Rempfer describes a stage where the first transistor pair 30 is N times larger than the second transistor pair 36. (Fig. 4, col. 3, lines 8-16). This pattern is repeated for additional amplification (Fig. 7; col. 3, lines 60-65). As a

consequence, at least one of the first and second transistors of pair 30 necessarily are larger than at least one of the third and fourth transistors of pair 36 of successive or preceding stages, and at least one of the third and fourth transistors necessarily are smaller than at least one of the first and second transistors of preceding or successive stages.

Whether the appellant intended to cover this arrangement with the appellant's claims is questionable; however, it is the applicants' burden to precisely define the invention. In re Morris, 127 F.3d 1048, 1056, 44 USPQ2d 1023, 1029 (Fed. Cir. 1997). The claims do not specify which "ones" are to be larger or smaller than "other ones," or that the transistors be larger or smaller than their "respective counterparts" in other stages. Accordingly, we agree with the examiner that the claimed arrangement is found within Rempfer.

The appellant argues that, for claims 27, 31, 35, and 39, a plurality of stages in non-feedback series cascade[2] are recited. Rempfer, it is stated, discloses a feedback series cascade. (Appeal Brief, page 9, lines 6-15). The examiner observes that Figure 7 illustrates an open switch which, when open, results in a non-feedback series cascade. (Examiner's Answer, page 8, lines

2 Again, our review of the specification reveals that it is unclear if the term "non-cascade," added in the new claims presented by the amendment of Paper 15, has supporting description in the as-filed specification. In the event of further prosecution of this application, the examiner and the appellant should

16-21). The appellant has not chosen to address this finding by the examiner in the reply brief.

We are in agreement with the examiner. Although Rempfer allows for periodic shorting, it appears that the principal operating mode of the cascade series is in non-feedback mode with occasional shorting (Rempfer, Fig 7; col. 3, line 65-col. 4, line 3). Accordingly, we are unpersuaded by this final argument.

Summary of Decision

The rejection of claims 1-4, 7-10, 13-16, 25, 27, 31, 35, and 39 under 35 U.S.C. §102(b) is sustained.

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address this issue.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

JAMESON LEE Administrative Patent Judge	)	
SALLY C. MEDLEY Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JAMES T. MOORE Administrative Patent Judge	)	

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