The opinion in support of the decision being entered today was **not** written for publication and is **not** precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte SANH D. TANG and RAJENDRA NARASIMHAN

_____

Appeal No. 2004-0633
Application No. 10/011,198

_____

ON BRIEF

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Before FLEMING, JEFFREY T. SMITH and PAWLIKOWSKI, **Administrative Patent Judges**.

PAWLIKOWSKI, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 31-47 and 56-58. A copy of each of the claims is set forth in the attached appendix.

The examiner relies upon the following references as evidence of unpatentability:

Yu et al. (Yu)	4,744,056	May 10, 1988
Cronin	5,539,255	Jul. 23, 1996
Ito	5,773,365	Jun. 30, 1998
Liu et al. (Liu)	6,015,749	Jun. 18, 2000

Claim 37 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Yu.

Claims 31-33 stand rejected under 35 U.S.C. § 103 as being obvious over Ito in view of Yu.

Claims 34-36 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cronin in view of Ito and Yu.

Claims 38-39 and 56-58 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cronin in view of Yu.

Claims 40 and 41 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cronin in view of Liu.

Claims 42 and 43 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cronin in view of Ito and Yu.

Claims 44-47 stand rejected under 35 U.S.C. § 103 as being unpatentable over Ito in view of Yu.

On page 2 of the brief, appellants group the claims into two groupings. Appellants group claim 37 into Group I, and appellants group claims 31-36, 38-47 and 56-58 into Group II. On page 2 of the brief, appellants indicate that the claims in Group II do not necessarily fall together. On page 1 of the reply brief, appellants refer to section 7 of the appeal brief, and also refer to page 10 of the appeal brief, in an effort to show that appellants have explained why the claims in Group II do not necessarily fall together. To the extent that any one claim is specifically and separately argued regarding patentability, we will consider such claim in this appeal. 37 CFR § 1.192(c)(7) and (8)(2003).

We have carefully reviewed appellants' brief and reply brief, the examiner's answer, and the applied references of record. This review has led us to conclude that the examiner's rejections are well-founded.

OPINION

I. The rejection of claim 37 under 35 U.S.C. § 102(b) as being anticipated by Yu

The critical issue in this rejection is the meaning of the claimed phrase, "integrated structure", as recited in claim 37.

As an initial matter, we note that during patent examination, the pending claims must be interpreted as broadly as their terms reasonably allow. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 320, 322 (Fed. Cir. 1999). In determining the patentability of claims, the PTO gives claim language its "broadest reasonable interpretation" consistent with the specification and claims. In re Morris, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997)(citations omitted).

Appellants argue that claim 37 requires at least one integrated structure comprising a first interconnect and an electrical connector. Appellants argue that Yu is different from this claimed subject matter because Yu combines two discrete structures, metal-1 conductor and the metal-2 conductor. Brief, page 3. In the reply brief, appellants continue to argue that the meaning given by the examiner regarding the term "integrated" is contrary to the suggested definition in the specification. Appellants continue to argue that the specification provides a sufficient definition for the term "integrated" and, hence, there is no need for the examiner's attempts to derive a plain meaning. Finally, on page 4 of the reply brief, appellants refer to Figures 6a, 7a, 8a, 12, and 18 of the specification to support a definition of "integrated" that is consistent with the specification's use of the term "integral".

On page 14 of the answer, the examiner states that contrary to appellants' assertion that the specification gives a special meaning to the term "integrated structure", there does not appear to be any explicit definition of the term "integrated structure." The examiner states that MPEP § 2111.01 states that when a term is not defined in the specification, the words of a claim must be given their plain meaning. The examiner states that in the final rejection of Paper No. 7, it was stated that "integrated" could be interpreted to mean "united". The examiner states that although no support for this definition was provided to the appellants, the examiner states that he used a dictionary definition. Answer, page 14. The examiner states that in view of the plain meaning of the claimed phrase "integrated structure", the structure disclosed by Yu, in Figure 6, showing a metal-1 connected (i.e., united) to metal-2, teaches this aspect of the claimed subject matter. Answer, page 14.

Hence, the meaning of the phrase "integrated structure" is in dispute.

We have carefully reviewed the entire specification in an effort to ascertain the meaning of the phrase an "integrated structure", as recited claim 37. This review is summarized below.

We refer to paragraphs [0022], [0026], [0031] of appellants' specification. These paragraphs indicate that when an "integral" plug is formed, such is formed in a manner as described, for example, in making conductive structures 120 and 122 as shown in Figure 4 and Figure 5. That is, a conductive material is deposited in a trench, as shown in Figure 4, and the resulting conductive structures 120, 122 are formed as shown in

Figure 5. The conductive structures 120, 122 can be made of the same metal, and result from the same metal deposition step, indicated by the "M1" designation, shown in Figure 5. The deposition process continues at least until the trenches are filled. Any metal deposited onto the top of insulation 26 can be removed through etching or by way of planarization techniques. The resulting conductive structures 120, 122 serve as interconnects or other conductive lines or paths. In addition, the conductive structures 120, 122 also provide conductive material for plugs that may be desired anywhere along those paths. Further, because such plugs will be defined along with the interconnects, the result will be a continuous and homogeneous electrically conductive structure including one part extending from one surface 24 to a more elevated surface 132, where other interconnects could be formed. See paragraph [0026] at the top of page 9 of the specification. Hence, it is clear that M1 shown in Figure 5 is the continuous and homogeneous electrically conductive structure, which includes interconnect site 124 and plug 128.

Also, in paragraph [0037], at the bottom of page 13 of appellants' specification, the specification describes Figure 18. Here, the recessed areas of openings 510 are filled with oxide 526. Oxide 526 can be etched back, as can the BPSG 508 in order to better expose the "plugs" included as an integral part of the conductive material 522 in openings 512, 514, and 516. Here again, is an example of the meaning of an "integral" part of the conductive material 522 shown in Figure 18.

Also, there are several places in the specification that the word "integral" can be found. This word is found in [0012] on page 4 the specification, the phrase "integral plugs" is

found in paragraph [0031] on page 11 of the specification, and, finally, the phrase "integral part" is found in paragraph [0037] on page 13 of the specification.

The above discussion of the parts of the specification are now considered with regard to the subject matter of claim 37, as follows. Claim 37 recites:

> 37. A portion of a memory array, comprising at least one integrated structure comprising a first interconnect within said memory array and an electrical connector extending upward from said interconnect.

Because of the claimed phrase "at least one integrated structure", claim 37 is open to multiple such structures. We find that layer metal-1 of Yu can be one integrated structure, and that layer metal-2 of Yu can be another integrated structure. Each of these layers is formed by a one-step metal deposition process. See column 6, lines 40-42, column 7, lines 34-35, and Figure 6 of Yu. Hence, as discussed above in regard to appellants' specification, layer metal-1 is formed by a one-step metal deposition process. Hence, it can be an M1 structure. Likewise, layer metal-2 can be such a structure. In this way, we agree with the examiner's anticipation rejection.

Therefore, we affirm the 35 U.S.C. § 102(b) rejection of claim 37.

II. <u>The 35 U.S.C. § 103 rejection of claims 31, 32, and 33 as being obvious over Ito in view of Yu</u>

On page 13 of the brief, appellants state that this rejection fails because of the conflicts between Ito and Yu as discussed in the brief. Beginning on page 9 of the brief, appellants discuss conflicts between Ito and Yu. On page 10 of

the brief, appellants state that Ito addresses a "stud up" structures that extends upward from an interconnect. Appellants state that in contrast, Yu focuses on how its metal-2 line must extend downward toward the drain of Yu's substrate. Appellants state that Ito touts the benefits of a damascene process used to form an interconnect. Appellants state that this is yet another conflict with Yu. At the bottom of page 10 of the brief, appellants state that Ito criticizes the non-damascene method of forming wiring and a projection as resulting in different resist layer thicknesses. At the top of page 11 of the brief, appellants state that, to the contrary, it is a non-damascene process that Yu proposes in forming its metal-2 line, a component that is arguably analogous to Ito's wiring.

On pages 4-5 of the answer, the examiner's position is that Ito basically sets forth the subject matter of claims 31-33[1], except that Ito does not expressly teach using the multilayer structure within a memory structure, which is a limitation of claim 31. The examiner relies upon Yu for disclosing memory cells of a random access memory that utilize multilayer wiring to connect to underlying field effect transistors. Answer, page 4. Appellants also do not dispute the examiner's findings with regard to Yu (that Yu establishes that is generally known in the art to use multilayer wirings in making electrical connections to random access memory).

In view of the above, it is the examiner's position that the multilayer wiring structure of Ito is suitable for a random access memory. Thus, the teachings relied upon by the examiner do not involve interchanging one of the process steps of Ito with one of the process steps of Yu, for example, such that the

[1] Appellants do not dispute these findings made by the examiner.

alleged conflicts that appellants discuss, are relevant. We therefore are not persuaded by appellants' arguments in this regard. Furthermore, we observe that Ito's multilayer structure is used for making a "semiconductor device". See column 1, lines 6-10 of Ito. Appellants have not directed us to evidence that the multilayer structure of Ito is not suitable for making the memory device.

In view of the above, we therefore affirm the 35 U.S.C. § 103 rejection of claims 31, 32, and 33.

III. The 35 U.S.C. § 103 rejection of claims 34, 35, and 36 as being obvious of Cronin in view of Ito and Yu

Appellants discuss this rejection on pages 9-11 of the brief. Here, appellants allege that there are conflicts between Cronin, Ito and Yu. We refer to the above-discussed rejection with regard to our determinations with regard to appellants' comments on the combination of Ito and Yu. We also provide the following.

With regard to Cronin, appellants argue that Cronin forms a stud-down with a single edge through thick insulation and with a single metal deposition, whereas Yu proposes building up the contact level by requiring a plurality of thin insulating layers in a plurality of conductive fill steps for those holes. Brief, page 10. Appellants state that Cronin touts the benefits of a damascene process and that this conflicts with Yu because Yu utilizes a non-damascene process. Brief, pages 10-11.

In view of the above, appellants present the same type of argument as presented with regard to the combination of Ito and Yu. Hence, for the very same reasons, discussed, supra, we are unpersuaded.

Furthermore, we incorporate the examiner's position on this rejection as set forth on pages 5-7 of the answer, as our own. On page 6 of the answer, the examiner recognizes that Cronin does not expressly teach or suggest two interconnects coupled through a plug as required by claim 34. The examiner relies upon Ito for teaching a wiring structure with two overlapping aluminum wire layers 25 and 30, electrically coupled through a columnar projection 26, that is integral to the lower wiring layer. Answer, page 6. The examiner states that it would have been obvious to have modified the teachings of Cronin by including an overlapping interconnect electrically coupled to an underlying interconnect as taught by Ito in order to provide electrical contact between the two metallization levels. The examiner relies upon Yu for teaching memory cells of a random access memory that utilizes interconnects. The examiner states that Yu therefore shows that it is known in the art to use interconnects in a random access memory for a memory cell.

Appellants do not argue any conflict between the process in Cronin and Ito. Appellants argue a conflict between Ito and Yu, and between Cronin and Yu. We have already addressed the alleged conflicts between Ito and Yu. For the same reasons, we are not persuaded by appellants' asserted conflicts between Cronin and Yu. The examiner is simply relying on Yu for showing that it is generally known in the art that memory cells of a random access memory utilize interconnects to connect to underlying field effect transistors, which appellants do not dispute.

With regard to Cronin in view of Ito, the issue is whether one of ordinary skill in the art would have been motivated to utilize a plug to connect the interconnect lines of Cronin.

Appellants admit that Ito does address a component analogous to Cronin's stud-up and that both references address how such a structure extends upward from an interconnect. Brief, page 10. Appellants also state that both Ito and Cronin taught the benefits of a damascene process used to form an interconnect. Hence, appellants acknowledge the similarities in the processes between Ito and Cronin. As stated by the examiner at the bottom of page 6 of the answer, Ito provides an alternative way of connecting two interconnects by utilizing a plug. Appellants have not argued that incorporation of this alternative way of connecting two interconnects cannot be accomplished in Cronin in view of the suggestions found in Ito.

In view of the above, we therefore affirm the 35 U.S.C. § 103 of claims 34, 35, and 36 as being obvious over Cronin view of Ito and Yu.

IV. <u>The 35 U.S.C. § 103 rejection of claims 38, 39, 56, 57, and 58 as being obvious over Cronin in view of Yu</u>

The examiner's position in this rejection is set forth on pages 7-8 of the answer.

Appellants' position is the same as discussed above with regard to Cronin and Yu. See pages 9-13 of the brief. Again, appellants do not dispute the examiner's findings with regard to Cronin. Appellants simply argue alleged conflicts between Cronin and Yu.

We emphasize that such conflicts are not material with regard to how the examiner combined the teachings of these references. Yu teaches that it is generally known in the art that a memory cell of a random access memory utilizes interconnects to connect to underlying field effect transistors.

Appellants do not dispute this finding. Utilizing the interconnect structure of Cronin for a memory structure would therefore have been obvious in view of Yu, for the reasons discussed, supra.

In view of the above, we affirm the 35 U.S.C. § 103 rejection of Claims 38, 39, 56, 57, and 58 under 35 U.S.C. § 103 as being obvious over Cronin in view of Yu.

V. Claims 40 and 41 under 35 U.S.C. § 103 as being obvious over Cronin in view of Liu

The examiner's position for this rejection is set forth on pages 9-10 of the answer. The examiner makes findings with regard to Cronin, and states that Cronin lacks the limitation set forth in claim 40 regarding the barrier liner layer, and the limitation set forth in claim 41 regarding the adhesion liner layer.

The examiner relies upon Liu for teaching use of a copper interconnect structure lined with a titanium nitride barrier layer, and a copper germanium adhesion layer.

The examiner states that it would have obvious to have modified the teachings of Cronin by using the barrier layers taught by Liu to prevent the diffusion of copper into the surrounding insulating layers and/or semiconductor regions. Answer, page 10.

On pages 4-9 of the brief, appellants argue alleged conflicts between Cronin and Liu. Appellants emphasize these conflicts on page 7 of the reply brief. Appellants argue that Cronin teaches placing a copper interconnect directly on a supporting insulating layer, whereas Liu teaches certain barrier layers to prevent the diffusion of copper, and utilizes certain

adhesion layers to improve adherence between the copper and the barrier layer.

On page 6 of the brief, appellants also argue that Cronin allows for a stud-down structure whereas Liu focuses on devices and phenomena underlying the interconnect. We are not convinced by appellants' asserted conflicts between Cronin and Liu.

Liu teaches the benefits of utilizing barrier and adhesion layers when connecting a copper interconnect to a surrounding structure. Certainly, one of ordinary skill in the art wanting to improve upon the structure of Cronin would have found it obvious to have utilized the teachings of Liu to do so for the reasons discussed by the examiner on page 10 of the answer.

In view of the above, we affirm the 35 U.S.C. § 103 rejection of claims 40 and 41 under 35 U.S.C. § 103 as being obvious of Cronin in view of Liu.

VI. The 35 U.S.C. § 103 rejection of claims 42 and 43 as being obvious over Cronin in view of Ito and Yu

The examiner's position for this rejection is set forth on pages 10-12 of the answer. The examiner states that although Cronin does teach additional levels of metallization with interconnection lines that have integral stud-up protrusions, Cronin does not expressly teach or suggest an upper interconnect in contact with the stud-up protrusion of the lower interconnect. The examiner also states that although Cronin recognizes that conductive level 12 can be representative of any type of active device, Cronin does not state that the interconnect structure is part of a memory apparatus.

The examiner relies upon Ito for teaching a wiring structure with two overlapping aluminum wiring layers

electrically coupled through a columnar protrusion that is integral to the lower wiring layer, and the examiner relies upon Yu for teaching memory cells of a random access memory that include interconnects formed over and connected to field effect transistors. Answer, page 12.

Appellants provide the same arguments that were provided regarding the references of Cronin, Ito and Yu, discussed, supra. See the brief, pages 9-13.

For the same reasons, therefore, we are not convinced by appellants' arguments regarding the alleged conflicts between Cronin and Yu, and between Ito and Yu.

In view of the above, we therefore affirm the 35 U.S.C. § 103 rejection of claims 42 and 43 under 35 U.S.C. § 103 as being obvious over Cronin in view Ito and Yu.

VII. The rejection of claims 44-47 under 35 U.S.C. § 103 as being obvious over Ito in view of Yu

The examiner's position for this rejection is set forth on pages 12 and 13 of the answer.

Appellants again apply the same arguments set forth on pages 9-13 of the brief regarding alleged conflicts between Ito and Yu.

For the very same reasons, therefore, as discussed supra, we are not convinced by the alleged conflicts between Ito and Yu.

Accordingly, we affirm the 35 U.S.C. § 103 rejection of claims 44-47 under 35 U.S.C. § 103 as being obvious over Ito in view of Yu.

VIII. Conclusion

Each of the prior art rejections is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

MICHAEL R. FLEMING Administrative Patent Judge	)
JEFFREY T. SMITH Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
BEVERLY A. PAWLIKOWSKI Administrative Patent Judge	)

BAP/sld

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Appendix

31. A system of interconnects for a memory structure, comprising:

a first interconnect within said memory structure;

a second interconnect coupled to said first interconnect through a plug, wherein said second interconnect and said plug define an integral structure;

a first insulator next to said second interconnect and said plug, said first insulator having a height in at least one area generally equal to a combined height of said second interconnect and said plug; and

a second insulator next to said plug, said second insulator having a height equal to a height of said plug.

32. The system in claim 31, wherein at least a portion of said second interconnect is under said first interconnect.

33. The system in claim 32, wherein said portion of said second interconnect is coupled to said first interconnect through said plug.

34. A system of interconnects for a memory structure, comprising:

a first interconnect within said memory structure; and

a second interconnect coupled to said first interconnect through a plug, wherein said second interconnect and said plug define an integral structure, wherein at least a portion of said second interconnect is under said first interconnect, and

wherein said portion of said interconnects to coupled to said first interconnect through said plug, and

a third interconnect laterally contacting a first insulator and at least partially isolated from said first interconnect by a second insulator.

35. The system in claim 34, wherein said second interconnect laterally contacts said first insulator.

36. The system in claim 35, wherein said second insulator laterally contacts said plug, and wherein said second insulator is over a part of said second interconnect.

37. A portion of a memory array, comprising at least one integrated structure comprising a first interconnect within said memory array and an electrical connector extending upward from said interconnect.

38. A portion of a memory device comprising:
at least two portions of insulation defining:
a first opening within said memory device, defining:
a first plug site, and
a first interconnect site in communication with said first plug site,
wherein said first plug site and said first interconnect site are filled with a continuous amount of conductive material; and
a second opening lateral to said first opening, said second opening defining:
a second plug site filled with at least one portion of said at least two portions of insulation, and
a second interconnect site in communication with said second plug site, wherein said second interconnect site is filled with said conductive material.

39. A level of interconnects for a memory device, comprising:
a layer of insulation defining a plurality of trenches within said memory device, wherein each trench of said plurality defines a lower portion and an upper portion, and wherein:
said lower portion is filled with metal,
said metal extends up into at least one area of said upper portion, and
said upper portion is filled with oxide except in said at least one area.

40. A level of interconnects for a semiconductor device, comprising:

a layer of insulation defining a plurality of trenches within said semiconductor device,

wherein each trench of said plurality defines a lower portion and an upper portion, and

wherein:

said lower portion is filled with metal,

said metal extends up into at least one area of said upper portion,

said upper portion is filled with oxide except in said at least one area, and

said each trench is lined with a barrier layer.

41. The level of interconnects in claim 39, wherein said each trench is lined with and adhesion layer.

42. A multi-layer interconnects structure for a memory apparatus, comprising:

a first layer of insulation forming a part of said memory apparatus;

a second layer of insulation over said first layer;

a first conductive path within said first layer of insulation, wherein said first conductive path comprises a first integral plug extending toward said second layer;

a discrete portion of insulation within said first layer, over said first conductive path, and under said second layer of insulation; and

a second conductive path within said second layer of insulation, wherein said second conductive path contacts said first plug.

43. The multi-layer interconnects structure of claim 42, wherein said second layer of insulation has a top, and wherein said second conductive path comprises a second integral plug extending toward said top.

44. A memory device comprising:

a first surface of memory device;

a first conductive element on said first surface;
a second surface below said first surface; and
a second conductive element on said second surface, wherein said second conductive element comprises a first part extending to said first conductive element and a second part integral to said first part and recessed from said first surface;
a first insulator lateral to said first part and said part in a first area next to said second conductive element; and
a second insulator lateral to said first part in a second area next to said second conductive element.

45. A memory device comprising:
a first surface of said memory device;
a first conductive element on said first surface;
a second surface below said first surface;
a second conductive element on said second surface, wherein said second conductive element comprises a first part extending to said first conductive element and a second part integral to said first part and recessed from said first surface;
a first insulator lateral to said second conductive element; and
a second insulator above said second part of said second conductive element;
wherein a top of said first insulator and a top of said second insulator define said first surface.

46. The memory device in claim 45, wherein said first conductive element is a conductive line.

47. The memory device in claim 45, wherein said second conductive element is an interconnect.

56. A multi-level circuit structure, comprising:
a first part of said circuit structure positioned in a lower level of a memory device and isolated from a higher level of said device; and
a second part of said circuit structure seamlessly coupled to said first part, wherein said second part extends to said higher level.

57. The structure in claim 56, wherein said first part and said second part are metal.

58. A multi-axial memory structure, comprising:

a first part of memory structure extending primarily along a first axis;

a second part of said memory structure integral to said first part, wherein said second part extends upward from said first part primarily along a second axis perpendicular to said first axis.