The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GLEN D. WILK,
ROBERT M. WALLACE,
JOHN M. ANTHONY
and PAUL MCINTYRE

Appeal No. 2004-0652
Application 09/396,642

ON BRIEF

Before FRANKFORT, STAAB, and MCQUADE, Administrative Patent Judges.

MCQUADE, Administrative Patent Judge.

DECISION ON APPEAL

Glen D. Wilk et al. originally took this appeal from the final rejection (Paper No. 7) of claims 1 through 12. Upon consideration of the appellants' main brief (Paper No. 9), the examiner issued an Office action (Paper No. 10) reopening prosecution and entering superseding rejections of the claims. Pursuant to 37 CFR § 1.193(b)(2)(ii), the appellants filed a supplemental brief (Paper No. 11) and requested that the appeal be reinstated. Implicitly denying this request, the examiner issued another Office action (Paper No. 12) entering further

superseding rejections of the claims. In response, the appellants filed a second supplemental brief (Paper No. 13) and again requested that the appeal be reinstated. The examiner then entered an answer (Paper No. 14), noted a reply brief (Paper No. 15) filed by the appellants and forwarded the application to this Board for review of the current rejections of claims 1 through 12. Claims 13 through 15, the only other claims pending in the application, stand withdrawn from consideration.

THE INVENTION

The invention relates to “semiconductor device fabrication and processing” (specification, page 1). Representative claims 1 and 9 read as follows:

1. A method of forming an electrically conductive structure insulatively spaced from a second structure, said method comprising the steps of:
providing said second structure;
forming an electrically insulative layer on said second structure;
forming on said electrically insulative layer and spaced form [sic, from] said second structure an unoxidized electrically conductive structure of a material that remains substantially conductive in the oxidized state; and
then subjecting said electrically conductive structure and said electrically insulative layer to an ozone containing atmosphere for a duration of time and at a first temperature sufficient to oxidize said unoxidized electrically conductive structure.

9. A method of forming a capacitor over a semiconductor substrate, said method comprising the steps of:
providing a first electrically conductive electrode on said semiconductor substrate;

forming a dielectric layer on said first electrically conductive electrode comprised of a first conductive material;

forming on said dielectric layer a second unoxidized electrically conductive electrode comprised of a second electrically conductive material which remains electrically conductive in the oxidized state; and

then oxidizing said second electrically conductive material by subjecting said second electrically conductive material and said dielectric layer to an ozone-containing atmosphere for a period of time greater than 20 minutes but less than 70 minutes.

THE PRIOR ART

The references relied on by the examiner to support the rejections on appeal are:

Wong	5,423,944	Jun. 13, 1995
Nishioka et al. (Nishioka)	5,554,564	Sep. 10, 1996

THE REJECTIONS

Claims 1, 2, 4, 5 and 7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nishioka.

Claims 3 and 6 through 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishioka in view of Wong.

Attention is directed to the appellants' briefs (Paper Nos. 9, 11, 13 and 15) and to the examiner's answer (Paper No. 14) for the respective positions of the appellants and the examiner regarding the merits of these rejections.

DISCUSSION

I. The 35 U.S.C. § 102(b) rejection of claims 1, 2, 4, 5 and 7 as being anticipated by Nishioka

Nishioka pertains to methods for forming capacitors containing materials having high dielectric constants. In general, the capacitors comprise a silicon semiconductor substrate 30, an insulative SiO_2 layer 32 overlying the substrate, a $TiSi_2$/poly-Si plug 34 providing electrical connection through the SiO_2 layer, a lower electrode consisting of a conductive adhesion layer 36 or 46 of either TiN (Figures 1 through 4) or Ru (Figures 5 through 8) deposited on the SiO_2 layer and a Pt layer 38 overlying the adhesion layer, a high dielectric constant BST layer 42 deposited over the lower electrode, and an upper electrode consisting of a Pt layer 44 overlying the BST layer. In order to minimize expansion and cracking of the BST layer 42 during its formation, Nishioka deposits the respective adhesion layers in a substantially unoxidized state and then pre-oxidizes their sidewalls to reduce any further oxidation and expansion during the BST layer deposition (see column 4, lines 39 through 63). The pre-oxidation step forms a non-conductive TiO_2 sidewall 40 on the TiN adhesion layer 36 and a conductive RuO_2 sidewall 50 on the Ru adhesion layer 46. With regard the pre-oxidation of the TiN

adhesion layer 36, Nishioka teaches that "[t]he structure is then annealed in a diluted oxygen (5%O_2 in N_2) gas at 650°C. to form TiO_2 sidewall 40 as shown in FIG. 2 . . . [or] [a]lternatively, ozone could be used for annealing . . . [or] [a]lternatively, the structure could be annealed at a lower temperature (e.g. 600°C.)" (column 5, lines 56 through 62). As for the pre-oxidation of the Ru adhesion layer 46, Nishioka teaches that "[t]he structure is then annealed in an oxygen containing atmosphere to form RuO_2 sidewall 50 as shown in FIG. 6" (column 6, lines 26 and 27).

Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984). In other words, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. Scripps Clinic & Research Found. v. Genentech Inc., 927 F.2d 1565, 1576, 18 USPQ2d 1001, 1010 (Fed. Cir. 1991). It is not necessary that the reference teach what the subject application teaches, but only that the claim read on something disclosed in the reference, i.e., that all of the limitations in the claim be found in or fully met by the reference. Kalman v.

Kimberly Clark Corp., 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 (1984).

In rejecting claims 1, 2, 4, 5 and 7, the examiner focuses on Nishioka's disclosure of the Ru adhesion layer embodiment illustrated in Figures 5 through 8. The determination by the examiner that this disclosure is anticipatory is well founded with respect to the subject matter recited in claims 1, 2, 5 and 7, but not with respect to the subject matter recited in claim 4.

Using the language in claim 1 as a guide, and notwithstanding the appellants' arguments to the contrary, Nishioka discloses a method of forming an electrically conductive structure insulatively spaced from a second structure (see Nishioka's Figures 5 through 8), which method comprises the steps of: providing said second structure (Nishioka's silicon semiconductor substrate 30); forming an electrically insulative layer (Nishioka's insulative SiO_2 layer 32) on said second structure; forming on said electrically insulative layer and spaced from said second structure an unoxidized electrically conductive structure (Nishioka' conductive Ru adhesion layer 46) of a material that remains substantially conductive in the oxidized state (conductive RuO_2); and then subjecting said electrically conductive structure and said electrically

insulative layer to an ozone-containing atmosphere for a duration of time and at a first temperature sufficient to oxidize said unoxidized electrically conductive structure (see Nishioka at column 5, lines 56 through 62; and column 6, lines 26 and 27). With regard to this last step, although Nishioka explicitly mentions ozone only in connection with the annealing and oxidation of the conductive TiN adhesion layer 36, a fair reading of the reference as a whole indicates that a person of ordinary skill in the art would view Nishioka's broad statement that the conductive Ru adhesion layer 46 is annealed and oxidized in an oxygen containing atmosphere as intending to encompass the same conditions expressed in conjunction with the corresponding and directly related TiN annealing and oxidation step. These conditions include the use of ozone, which is of course an oxygen containing atmosphere, and a 600°C. annealing temperature.

Furthermore, Nishioka's conductive Ru adhesion layer 46 meets the recitation in dependent claim 2 that the electrically conductive structure is comprised of a material selected from the group consisting of: Ir, Ru, Rh and any combination thereof, Nishioka's insulative SiO_2 layer 32 (an oxide) meets the recitation in dependent claim 5 that the electrically insulative layer is comprised of a material selected from the group

consisting of: tantalum pentoxide, BST, PZT, a silicate, an oxide, a nitride, a combination thereof and a stack of one or more thereof, and Nishioka's teaching that the annealing and oxidation step can take place at a temperature of 600°C. meets the recitation in claim 7 that the first temperature is around 20 to 600 C.

On the other hand, Nishioka's description of the use of ozone in the annealing and oxidation step is not specific enough to meet the recitation in dependent claim 4 of "remotely" forming the ozone.

In light of the foregoing, we shall sustain the standing 35 U.S.C. § 102(b) rejection of claims 1, 2, 4, 5 and 7 as being anticipated by Nishioka with respect to claims 1, 2, 5 and 7, but not with respect to claim 4.

<u>II. The 35 U.S.C. § 103(a) rejection of claims 3 and 6 through 12 as being unpatentable over Nishioka in view of Wong</u>

Wong discloses a method for etching a silicon wafer using hydrogen fluoride and water vapor combined with ozone. Of interest is Wong's teaching that the ozone may be produced (1) in a remote plasma generator or (2) in the etching apparatus itself using ultraviolet excitation (see column 2, lines 49 through 57).

In neither case, however, is the ozone formed over the subject silicon wafer.[1]

As explained above, Nishioka meets the temperature limitation in dependent claim 7. We shall therefore sustain the standing 35 U.S.C. § 103(a) rejection of claim 7 as being unpatentable over Nishioka in view of Wong, with the examiner's application of Wong here being harmless surplusage.

We shall not sustain, however, the standing 35 U.S.C. § 103(a) rejection of claims 3, 6 and 8 which depend from claim 1. The examiner has not cogently explained, and it is not apparent, how or why the combined teachings of Nishioka and Wong would have suggested performing Nishioka's annealing and oxidation step with an ozone-containing atmosphere formed over the electrically conductive structure and the electrically insulative layer as recited in claim 3, for more than 20 minutes but less than 70 minutes as recited in claim 6, or at a temperature around 400 to 500C as recited in claim 8.

We also shall not sustain the standing 35 U.S.C. § 103(a)

[1] In the event of further prosecution, the examiner should consider whether Nishioka, taken in combination with Wong's teaching of forming ozone at a location remote from where it is intended to be used, would have suggested the subject matter recited in claim 4, thereby warranting a § 103(a) rejection.

rejection of independent claim 9 and dependent claims 10 through 12 as being unpatentable over Nishioka in view of Wong.

As indicated above, claim 9 recites a method of forming a capacitor over a semiconductor substrate comprising, inter alia, the step of oxidizing the second electrically conductive material by subjecting it and the dielectric layer to an ozone-containing atmosphere for a period of time greater than 20 minutes but less than 70 minutes. In apparent recognition that Nishioka's oxidizing step is performed on an electrically conductive material that corresponds to the first, rather than the second, electrically conductive material recited in claim 9, the examiner appears to conclude (see page 4 in the answer) that it would have been obvious to simply interchange Nishioka's first electrically conductive layer (conductive Ru layer 46 and Pt layer 38) and second conductive layer (Pt layer 44). The combined teachings of Nishioka and Wong provide no suggestion for this modification which is completely inconsistent with the fair teachings of Nishioka or for the 20 to 70 minute time limitation.

SUMMARY

The decision of the examiner to reject claims 1 through 12 is affirmed with respect to claims 1, 2, 5 and 7, and reversed with respect to claims 3, 4, 6 and 8 through 12.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

CHARLES E. FRANKFORT Administrative Patent Judge	)	
	)	BOARD OF PATENT
	)	APPEALS AND
LAWRENCE J. STAAB Administrative Patent Judge	)	INTERFERENCES
JOHN P. MCQUADE Administrative Patent Judge	)	

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TEXAS INSTRUMENTS INCORPORATED
P. O. BOX 655474, M/S 3999
DALLAS, TX 75265