

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 29

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

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Ex parte CHAU CHIN LOW et al.

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Appeal No. 2004-0748  
Application No. 09/427,226

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ON BRIEF

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Before STAAB, NASE, and BAHR, Administrative Patent Judges.  
NASE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 to 7 and 11 to 16, which are all of the claims pending in this application.

We REVERSE.

BACKGROUND

The appellants' invention relates generally to methods and devices for increasing the density of integrated circuits (IC's) placed on a substrate such as a printed circuit board (PCB), and more particularly to methods and devices for stacking chips comprising surface mount technology (SMT) chip packages (specification, p. 1). A copy of the claims under appeal is set forth in the appendix to the appellants' brief.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

|           |           |               |
|-----------|-----------|---------------|
| Burns     | 5,484,959 | Jan. 16, 1996 |
| Buechele  | 5,768,772 | June 23, 1998 |
| Hacke     | 6,157,541 | Dec. 5, 2000  |
| Farnworth | 6,168,969 | Jan. 2, 2001  |

Claims 1, 2, 11 and 12 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Buechele.

Claims 3 to 5 and 15 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Hacke.

Claims 6, 7 and 16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Farnworth in view of Burns.

Claims 13 and 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hacke.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejections, we make reference to the final rejection (Paper No. 18, mailed May 30, 2002) and the answer (Paper No. 23, mailed January 30, 2003) for the examiner's complete reasoning in support of the rejections, and to the brief (Paper No. 22, filed October 22, 2002) for the appellants' arguments thereagainst.

#### OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the examiner. As a consequence of our review, we make the determinations which follow.

#### **The anticipation rejection based on Buechele**

We will not sustain the rejection of claims 1, 2, 11 and 12 under 35 U.S.C. § 102(e) as being anticipated by Buechele.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

Verdegaal Bros. Inc. v. Union Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir.), cert. denied, 484 U.S. 827 (1987). The inquiry as to whether a reference anticipates a claim must focus on what subject matter is encompassed by the claim and what subject matter is described by the reference. As set forth by the court in Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 (1984), it is only necessary for the claims to "'read on' something disclosed in the reference, i.e., all limitations of the claim are found in the reference, or 'fully met' by it."

Claims 1 and 2 on appeal read as follows:

1. A method of stacking chips by positioning at least two chip layers into an assembly fixture comprising a floor, each layer comprising at least one chip, the method comprising steps of:
  - (a) positioning a first chip layer directly on the floor;
  - (b) positioning a first spacer layer on the first chip layer;
  - (c) positioning at least one additional chip layer over the spacer layer;
  - (d) coupling the layers together; and
  - (e) removing the coupled layers from the assembly fixture, the coupled layers comprising at least one stacked device.
2. A stacked device made by the method of claim 1.

Buechele describes his invention with reference to an apparatus and preferred lamina transport mechanisms therein for automating a larger portion of the process for assembly of multi-layer ceramic (MLC) or other modular circuit packages. The apparatus includes a stacking/removal mechanism 100, a pin stacking assembly 120 and a floating stack head 130. As illustrated in Figure 4, three complete groups of lamina 302 have been stacked, separated and covered by separator plates 303 and mylar sheets 301. At this point, the entire pin stacking assembly 120 with the stacked lamina thereon can be removed from a mounting plate 118 of the stacking/removal mechanism 100 and transferred to a warm frame for establishing a uniform temperature for lamination and, in due course, to a lamination press and oven for lamination. After lamination, the lamina stack is removed from the pin stacking assembly 120.

The appellants argue (brief, pp. 3-4) that the limitation "each layer comprising at least one chip" is not met by Buechele. We agree. The appellants have defined (specification, p. 8) "chip" as "a package containing at least one die, the package having external contacts electrically coupled to at least some of electrically operative contacts of the at least one die." Thus, the IEEE definition applied by the examiner (final rejection, p. 5) cannot be used in this application. We have fully reviewed Buechele but fail to find any disclosure therein that the lamina 302 contain a "chip" as defined by the appellants. Accordingly, claims 1 and 2 are not anticipated by Buechele.

For the reasons set forth above, the decision of the examiner to reject claims 1 and 2, and claims 11 and 12 dependent thereon, under 35 U.S.C. § 102(e) as being anticipated by Buechele is reversed.

### **The anticipation rejection based on Hacke**

We will not sustain the rejection of claims 3 to 5 and 15 under 35 U.S.C. § 102(e) as being anticipated by Hacke.

Claims 3 and 5 on appeal read as follows:

3. A method of stacking similar, packaged first and second dies comprising steps of:
  - (a) mounting at least one of the first dies into a first package;
  - (b) installing several electrical conduits into the first package in a first conduit configuration;
  - (c) mounting at least one of the second dies into a second package;
  - (d) installing several electrical conduits into the second package in a second conduit configuration different from the first configuration; and
  - (e) electrically coupling the first package to the second package to form a stacked device.
  
5. A stacked device made by the method of claim 3.

Hacke teaches that two semiconductor memory chips are placed onto a flexible wiring and are shaped by simple folding of the flexible wiring about a central elastic line, into a space-efficient stack arrangement whose outer contacts are formed only at one marginal side. To form memory cards, a plurality of such stack arrangements can

be placed onto a simply constructed printed board. Figure 12 is a side view of one embodiment of the stack arrangement for two semiconductor memory chips, prior to the folding of the flexible carrier film and Figure 13 is a side view of that stack arrangement subsequent to the folding of the flexible carrier film. As shown in Figure 12, the stack arrangement includes a flexible carrier film TF2 and two semiconductor memory chips HSC. Hacke teaches (column 5, line 56, to column 6, line 4) that:

All the inner terminals IA are placed on one side of the carrier film TF2. Essentially both groups of conductors also extend on this side, of which only the conductors L1 can be seen in FIG. 12. The individual conductors are fed to the other side of the carrier film TF2 via throughplatings D1 only in the case of a transposition. It can also be seen in FIG. 12 that the two semiconductor memory chips HSC are bonded to the allocated inner terminals IA in face-down position. It is important that all the conductors are fed together via the strip-shaped bonding region referenced KB2, so that the outer contacts AK are formed subsequent to the folding about the elastic line BL2 according to FIG. 13. Given the folding direction indicated by an arrow PF1 in FIG. 12, in the finished stack arrangement according to FIG. 13, the two semiconductor memory chips HSC are situated on opposite outer sides of the stack.

The appellants argue (brief, pp. 4-5) that Hacke does not disclose mounting a first die into a first package; mounting a second die into a second package; and electrically coupling the first package to the second package to form a stacked device. We agree. In our view, the stack arrangement for two semiconductor memory chips shown in Figure 12 of Hacke constitutes only a single package and not first and second packages especially since the two semiconductor memory chips HSC are connected together prior to folding into the finished stack arrangement. In that regard, the

conductors L1 which are fed together via the strip-shaped bonding region KB2 interconnect the two semiconductor memory chips HSC so that the outer contacts AK are formed subsequent to the folding. Accordingly, claims 3 and 5 are not anticipated by Hacke.

For the reasons set forth above, the decision of the examiner to reject claims 3 and 5, and claims 4 and 15 dependent thereon, under 35 U.S.C. § 102(e) as being anticipated by Hacke is reversed.

#### **The obviousness rejection based on Hacke**

We will not sustain the rejection of dependent claims 13 and 14 under 35 U.S.C. § 103 as being unpatentable over Hacke for the reasons set forth above with respect to claim 3. In addition, we note that the Official Notice taken by the examiner in the final rejection (pp. 4-5) was timely challenged by the appellants (brief, p. 7). When the appellants seasonably challenge a factual assertion as not properly officially noticed or not properly based upon common knowledge, the examiner must support the finding with adequate evidence. See In re Chevenard, 139 F.2d 711, 713, 60 USPQ 239, 241 (CCPA 1943) and MPEP 2144.03. This was not done in this instance.

### **The obviousness rejection based on Farnworth and Burns**

We will not sustain the rejection of claims 6, 7 and 16 under 35 U.S.C. § 103 as being unpatentable over Farnworth in view of Burns.

Claim 6 reads as follows:

A method of making a stacked device comprising at least a first integrated circuit (IC) die and a second IC die, comprising steps of:

- (a) building a first IC chip by installing the first die in a first package;
- (b) building a second IC chip by installing the second die in a second package, the second die being identical to the first die, the second package being internally identical to the first package;
- (c) sealing the packages;
- (d) modifying the electrical characteristics of at least one of the chips; and
- (e) electrically coupling the first chip to the second chip to form a stacked device.

Farnworth's invention relates to semiconductor devices and associated integrated circuit configurations and, more particularly, to bare die configurations and stacked multi-chip (bare die) assemblies with chip-integral vertical connection circuitry and a method of fabricating such die and assemblies. Farnworth teaches (column 3, lines 26-45) that:

Each die of the preferred plurality is provided with vias to interconnect with dice above or below it or a carrier substrate, as the case may be. Vertically-aligned vias extending from the carrier substrate through each die to and through the uppermost die comprise a commonly-accessed conductive vertical pathway from the substrate to each die in the stack for such commonly-required functions as power, ground, I/O, CAS, RAS, etc. Discrete or individual vertical pathways for chip-selects extend to each of the various dice, so

that each die accesses the carrier substrate for commonly-required functions commonly and discrete functions individually. It is contemplated that dice to be employed in a stack may have the same or different components but a common via layout for easy superimposition. The overall circuit defined by the die stack may then be customized by the number and type of die employed and the use of laser-blown or electrically-blown fuse elements, as known in the art, incorporated in the die circuitry of each die. Thus, a via stack may be electrically connected to components at one die level, but not at those above or below, serving only at the other (unconnected) die levels as a bypass conductor.

Figures 1A, 1B and 1C of Farnworth depict an exemplary silicon die 10 with exemplary conductive vias 12 and 14. An epitaxial layer 20 is formed on active side 16. Active devices<sup>1</sup> 22 are superimposed on or immediately adjacent via 12. Passive devices<sup>2</sup> 23 (see Figure 3) may similarly be formed on die 10.

Figure 4 of Farnworth depicts an eight-die stack including dice 210a, 210b, 210c, 210d, 210e, 210f, 210g, and 210h mounted on and electrically connected to a carrier substrate 230. As can be seen schematically, a series of common-access via stacks 212a, 212b, 212c, 212d and 212e extend vertically through all eight dice and are accessed by each. A second series of discrete access via stacks 214a, 214b, 214c, 214d, 214e, 214f, 214g, and 214h provide an individual chipselect function to each die

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<sup>1</sup> Active devices may include any such devices known in the art such as diodes, transistors, and memory (ROM, PROM, EPROM, EEPROM, bubble, DRAM, SRAM) including subcomponents such as transistors, capacitors and fuses.

<sup>2</sup> Such as resistors, capacitors, fuses, etc.

in the stack. Several exemplary programmable blown or open fuse elements 260a, 260b and 260c are also depicted, such open fuse elements isolating a die above a certain level from a particular via stack. Thus, for example, a chip-select via for the base dice 210h may be isolated from the remaining seven (7) die above it. Other vias may similarly be isolated. Programmable antifuses may similarly be employed to selectively connect, rather than disconnect, conductors on and between dice. Several programmable activated or closed fuse elements are depicted at 264a, 264b, and 264c. Fuses and antifuses may, of course, be employed in combination on the same die and on adjacent dice.

Burns' invention relates to forming an improved package particularly suited for multiple-unit three-dimensional stacking. This improved package is fabricated by attaching a lead frame to an integrated circuit package in a manner that results in improved thermal transfer of heat from within the integrated circuit package and provides additional electrical conductors useful with addressing and communicating multiple package modules. Figure 20 relied upon by the examiner is an embodiment having four thin small outline package (TSOP) integrated circuit packages 22 stacked together and electrically and thermally interconnected through rails 70. Packages 22 are laminated to lead frames 27 and then the lead frames 27 are connected to the rails 70 by soldering, thermal compression bonding or any other suitable means.

In this rejection (final rejection, pp. 3-4) the examiner ascertained that Farnworth does not disclose (1) building a first IC chip by installing the first die in a first package; (2) building a second IC chip by installing the second die in a second package; and (3) sealing the packages. The examiner then concluded that it would have been obvious at the time of the invention to a person of skilled in the art to use the packaged dies of Burns with the method of making a stacked device of Farnworth "in order to easily electrically interconnect the individual packages using the lead frame leads, while also utilizing a sealed device."

The appellants argue (brief, pp. 5-6) that the applied prior art does not suggest the claimed subject matter. We agree. In our view, Burns provides no suggestion, teaching or motivation for a person of ordinary skill in the art at the time the invention was made to have modified Farnworth to arrive at the claimed invention. In that regard, Farnsworth, as noted above, is directed to bare die configurations and stacked multi-chip (bare die) assemblies with chip-integral vertical connection circuitry while Burns, as noted above, is directed to four TSOP integrated circuit packages 22 stacked together, and we discern no reason to combine these disparate teachings together. Obviousness is tested by "what the combined teachings of the references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). But it "cannot be established by combining the

teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). And "teachings of references can be combined only if there is some suggestion or incentive to do so." Id. Here, the prior art contains none. Instead, it appears to us that the examiner relied on hindsight in reaching his obviousness determination. However, our reviewing court has said, "To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." W. L. Gore & Assoc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). It is essential that "the decisionmaker forget what he or she has been taught . . . about the claimed invention and cast the mind back to the time the invention was made . . . to occupy the mind of one skilled in the art who is presented only with the references, and who is normally guided by the then-accepted wisdom in the art." Id.

For the reasons set forth above, the decision of the examiner to reject claim 6, and claims 7 and 16 dependent thereon, under 35 U.S.C. § 103 as being unpatentable over Farnworth in view of Burns is reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1 to 5, 11, 12 and 15 under 35 U.S.C. § 102(e) is reversed and the decision of the examiner to reject claims 6, 7, 13, 14 and 16 under 35 U.S.C. § 103 is reversed.

REVERSED

|                             |   |                 |
|-----------------------------|---|-----------------|
| LAWRENCE J. STAAB           | ) |                 |
| Administrative Patent Judge | ) |                 |
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|                             | ) | BOARD OF PATENT |
| JEFFREY V. NASE             | ) | APPEALS         |
| Administrative Patent Judge | ) | AND             |
|                             | ) | INTERFERENCES   |
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| JENNIFER D. BAHR            | ) |                 |
| Administrative Patent Judge | ) |                 |

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