The opinion in support of the decision being entered today was not written
for publication and is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte KIMBLE DONG et al.

Appeal No. 2004-1543
Application No. 09/303,991

ON BRIEF

Before ABRAMS, FLEMING, and NASE, Administrative Patent Judges.

NASE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 7 to 13. Claims 1 to 6 and 14, the only other claims pending in this application, have been withdrawn from consideration by the appellants (brief, p. 2).

We REVERSE.

BACKGROUND

The appellants' invention relates to CMOS image sensors and, more particularly, to a CMOS image sensor that can be used as part of a multiple-camera monitoring system (specification, p. 1). A copy of the claims under appeal is set forth in the appendix to the appellants' brief.

Claims 7 to 13 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,159,455[1] to Cox et al. (Cox) in view of U.S. Patent No. 5,144,445[2] to Higashitsutsumi and Official Notice .

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejection, we make reference to the answer (Paper No. 15, mailed July 16, 2003) and the supplemental answer (Paper No. 20, mailed November 19, 2003) for the examiner's complete reasoning in support of the rejection, and to the brief (Paper No. 19, filed August 22, 2003) and reply brief (Paper No. 21, filed November 25, 2003) for the appellants' arguments thereagainst.

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[1] Issued October 27, 1992.

[2] Issued September 1, 1992.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art, and to the respective positions articulated by the appellants and the examiner. Upon evaluation of all the evidence before us, it is our conclusion that the evidence adduced by the examiner is insufficient to establish a prima facie case of obviousness with respect to the claims under appeal. Accordingly, we will not sustain the examiner's rejection of claims 7 to 13 under 35 U.S.C. § 103. Our reasoning for this determination follows.

In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). A prima facie case of obviousness is established by presenting evidence that would have led one of ordinary skill in the art to combine the relevant teachings of the references to arrive at the claimed invention. See In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988) and In re Lintner, 458 F.2d 1013, 1016, 173 USPQ 560, 562 (CCPA 1972). Rejections based on 35 U.S.C. § 103 must rest on a factual basis with these facts being interpreted without hindsight reconstruction of the invention from the prior art. The examiner may not, because of doubt that the invention is patentable, resort to speculation, unfounded assumption or hindsight reconstruction to supply deficiencies in the factual basis for the

rejection. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968).

With this as background, we analyze the prior art applied by the examiner in the rejection of the claims on appeal.

Cox's invention provides an apparatus capable of producing an arbitrarily large number of video pixels without reducing the frame rate at which the apparatus can be operated. This objective is achieved by running multiple relatively small sensor arrays in parallel, thus providing a large number of pixels per video frame. These pixels are grouped into individual segments corresponding to the field of view of each of the small sensor arrays. Accordingly, each segment needs to be spliced together to form a contiguous ultra-high-resolution image. This splicing needs to take place at both the front and the rear end of the system. Multiple video cameras outputs must be spliced together to create a single ultra-high-resolution video signal such as an RS-343 real-time video signal. In this case, a scan converter is used which takes the incoming parallel video signals, digitizes them and feeds a memory array or buffer. This memory array can be read out in a high speed serial sequence while it is being fed by the incoming video. The digital data is then converted back to analog. Video sync signals are then added to the analog signal thus creating an RS-343 video signal.

Figure 8 of Cox shows an ultra-high-resolution multicamera device 41 having a plurality of tapered fiber-optic bundles 15 which have a machined or fused joint 42 therebetween in order to form a continuous image surface. The multicamera device 41 includes solid-state cameras 45 which are connected to receive the images input to the tapered fiber-optic bundles 15 and directed to the image sensor module 17. Cox teaches (column 3, lines 28) that the image sensor module 17 is typically a solid-state discrete element electro-optical scanner of the CCD, CID or MOS type, but may also be a conventional television camera tube. The video images received by the cameras 45 are transmitted via cable 46 to a scan converter 40 so that the video images can be spliced together to create an output which corresponds to a composite image 30 (see Figure 5b).

Figure 9 of Cox is a block diagram of the multicamera device 41 with the scan converter 40. The scan converter 40 includes an analog section 60, an A/D section 62, a timing section 64, a frame buffer section 66, and finally a video out section 68. Cox discloses (column 5, line 60, to column 8, line 6) the operation of the multicamera device 41 as follows:

> The image sensor modules 17 detect the bundle sub-images 16 and analog video signals are output via cables 46 to a buffer and clamp circuit 72 in the analog section 60. The analog video signals are synchronized to a system pixel clock 69 and clamped to a reference voltage before being output to an analog-to-digital (A/D) converter 76 in the A/D section 62, which converts the analog signals to digital video data. This digital video data is temporarily stored in

a buffer 77 before being read into one of two memory arrays 82 or 84 in the memory section 66. Memory addresses are assigned to each digital video datum by address generator 80 in the timing section 64. Once digital delay generators 86 are properly adjusted the memory addresses are assigned only to digital video data of interest, i.e. the digital video data corresponding to the horizontal and vertical deadzones are not assigned memory addresses and consequently are not read into either memory array 82 or 84. After an entire frame of digital video data is stored in either memory array 82 or 84, the digital data is read out of that memory array in the proper order so that this ordered digital video data is either displayed using new global addresses and a digital display or is digital-to-analog (D/A) converted resulting in a high-resolution analog video signal. This high resolution analog video signal can be displayed as the composite image 30 (without deadzones) using a high resolution TV monitor. The multicamera device in FIG. 9 will now be described in more detail.

A video gen-lock circuit 70 synchronizes the arrival of the analog video signals from the solid-state cameras 45 with respect to each corresponding horizontal sync pulse. The synchronization of the gen-lock circuits 70 and pixel clock 69 should ensure that the video signals on line 46 are synchronized. However, if additional synchronization, a buffer circuit 73 in the buffer and clamp circuit 72 could provide a delay mechanism for delaying the analog signal so that the video lines from all four cameras arrive at the A/D converter 76, consistently to within a fraction of one system pixel cycle. The buffer circuits would provide variable delays and outputs synchronized with the pixel clock. The system pixel clock 69 could be from one of the solid-state cameras 45 or an outside clock. The gen-lock circuit 70 also provides horizontal sync pulse information to the digital delay generator 86. The digital delay generator 86 then outputs delayed horizontal and vertical sync pulses to the address generator 80, which tell the address generator 80 when to begin generating memory addresses.

The buffer and clamp circuit 72 provides video voltage regulation so that the A/D conversion of the analog video signal is on an absolute level. The portion of the video line directly following the horizontal sync pulse must be clamped at a fixed voltage level corresponding to black for example. This is necessary because the A/D converter 76 in the A/D section 62 will eventually A/D convert the video signal using this fixed voltage level as a reference level. Without the buffer and clamp circuit 72 this reference voltage level will typically vary a few millivolts from line to line and camera to camera. The buffer circuit 73 and clamp circuit 74 in the buffer and clamp circuit 72 are standard buffer and clamp circuits.

The clamped and delayed video signal output from the buffer and clamp circuit 72 as well as the synchronizing signals output by the video gen-lock circuit 70 are input to the A/D section 62. The A/D converter 76 samples the output of the buffer and clamp circuit 72, N times where N corresponds to the number of pixels in a horizontal scan of the solid-state sensor array 17; typically N is somewhere in the range of 520 to 590. The analog voltage levels V1, V2, V3 . . ., VN shown in FIG. 4d are all converted to digital signals, (typically 8 bits). In order to obtain real time high resolution images the A/D converter 76 is preferably a flash converter. The A/D conversion process is clocked at a rate corresponding to the system pixel clock 69.

The digital video data output from the A/D converter 76 is then input to a buffer 77 which holds that digital video data so that the address generator 80 can feed address lines into memory arrays 82 and 84 according to the system pixel clock 69 and/or the horizontal and vertical sync pulses. The other circuit in the A/D section 62 is the digital delay generator 86. The digital delay generator 86 is connected to the video gen-lock circuit 70 which provides the digital delay generator 86 with horizontal and vertical sync pulse information. The digital delay generator 86 has some type of discrete level setting mechanism such as a thumb wheel switch. This thumb wheel switch can be used to delay the onset by the address generator 80 of loading addresses into the memory arrays 82 or 84. This delay actually can comprise two components. There can be a delay in terms of horizontal sync pulses after a vertical sync pulse for eliminating horizontal deadzones, and there can be a delay in terms of pixel clock pulses after a horizontal sync pulse to eliminate vertical deadzones. In other words, although the A/D converter 76 is continuously digitizing the video signal, the digitized video signals output by the buffer 77 are ignored by the address generator 80 until it is commanded to begin address generation and signal storage by the digital delay generator 86. This will effectively eliminate any digital video data corresponding to the horizontal and vertical deadzones and only digital video data without deadzones is stored in the memory arrays 82 and 84. This operation is controlled by observing the composite image on the high-resolution video monitor and turning the thumbwheel switches to adjust the horizontal and vertical delays until the deadzones are eliminated.

The timing section 64 sets up and loads the digital data output from the A/D section 62 into the memory arrays 82 and 84. The address generator 80 loads the digital words into their appropriate memory location in 82 or 84. The memory arrays 82 and 84 can be standard 120 nano-second dynamic random access memory or D-RAM. This slow memory can be used only if an

> inter-leaving scheme is used to store the digital words output from the timing section 64. Two memory arrays 82 and 84 are used so that a complete frame can be stored in each. It is necessary to completely assemble a frame of video before it can be read out. The two memory arrays 82 and 84 make it possible to write to one memory array while reading from the other memory array and vice versa. The parity select 88 determines when to write to or read from the memory arrays 82 and 84. Hence, although twice as much memory is used, using two memory arrays eliminates tearing of the composite image. A second advantage to using two memory arrays is that the memory arrays 82 and 84 can be shared with some type of processor such as an AT computer by using a bus 90. The digital video data can then be taken out via the bus 90 and printed to a laser printer or stored on an optical disc or used in any other digital image processing device.
>
> The final section of the scan converter 40 is the video out section 68. An address generator 92 provides a global address for a single frame corresponding to the composite video image 30. The address generator 92 also provides refresh to the memory arrays 82 and 84. A sync generator 94 provides an ultra-high-resolution sync signal for the single frame composite video image. It will be understood that address generator 92, sync generator 94 and D/A converter 98 are synchronized to the pixel clock of the high resolution video display, which is at least four times as fast as the pixel clock 69. FIGS. 10a and 10b demonstrate the order in which the address generator 92 would generate global addresses for outputting the digital video data stored in memory arrays 82 and 84 in order to produce the composite video image 30.

Higashitsutsumi's invention relates to a solid-state image pickup apparatus for supplying a video signal to a display unit. The object of Higashitsutsumi's invention was to eliminate the waste of the TV cameras in a solid-state image pickup apparatus and simplify the circuits for connecting the TV cameras so as to greatly reduce the cost. Figure 9 is a block diagram of an image pickup system using a plurality of solid-state image pickup apparatuses which are connected together and the images of the

respective solid-state image pickup apparatuses are simultaneously displayed on a TV monitor 127. Television cameras 121 to 124 each have a CCD solid-state image pickup device and respectively output video signals Y^1 to Y^4 for displaying the images reduced in size to ½ in the vertical and horizontal directions. Synchronizing signals SY^1 to SY^4 are supplied from a synchronizing signal generator 125 to the respective television cameras 121 to 124 for synchronizing the respective operations and setting the timings for vertical scanning and horizontal scanning at delays of V/2 and H/2. The video signals Y^1 to Y^4 are compounded into a new video signal Y^m by a composite video signal generator 126 and the composite video signal Y^m is supplied to a TV monitor 127. Thus, the images which correspond to the respective video signals Y^1 to Y^4 are simultaneously displayed on the reproducing screen of the TV monitor 127, as shown in Figure 11.

In addition to the teachings of Cox and Higashitsutsumi, the examiner took Official Notice that phase-locked loops are known to synchronize output clock signals by the use of incoming reference signals.

After the scope and content of the prior art are determined, the differences between the prior art and the claims at issue are to be ascertained. Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966).

Based on our analysis and review of Cox and claims 7 to 13, it is our opinion that the differences include (1) synchronizing the analog video outputs by providing a reference signal to phase-locked loop circuitry in at least one of the CMOS image sensors; and (2) maintaining the analog video outputs from the CMOS image sensors in analog format along the entire signal path from the CMOS image sensors to the display.

With regard to these differences, the examiner determined (final rejection, pp. 6-8) that at the time the invention was made it would have been obvious to one with ordinary skill in the art to have modified Cox to (1) use a phase-locked loop as the pixel clock; and (2) maintain the analog video outputs from the CMOS image sensors in analog format along the entire signal path from the CMOS image sensors to the display as taught by Higashitsutsumi. We do not agree.

Most if not all inventions arise from a combination of old elements. See In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed. Cir. 1998). Thus, every element of a claimed invention may often be found in the prior art. See id. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. See id. Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination

that was made by the appellants. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). In addition, the teaching, motivation or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. See WMS Gaming, Inc. v. International Game Tech., 184 F.3d 1339, 1355, 51 USPQ2d 1385, 1397 (Fed. Cir. 1999). The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. See In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981) (and cases cited therein). Whether the examiner relies on an express or an implicit showing, the examiner must provide particular findings related thereto. See Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617. Broad conclusory statements standing alone are not "evidence." Id. When an examiner relies on general knowledge to negate patentability, that knowledge must be articulated and placed on the record. See In re Lee, 277 F.3d 1338, 1342-45, 61 USPQ2d 1430, 1433-35 (Fed. Cir. 2002).

In this case, while phase-locked loop circuitry is known, we fail to find any motivation, suggestion or teaching in the applied prior art that would have made it obvious at the time the invention was made to a person of ordinary skill in the art to have modified Cox to use phase-locked loop circuitry as the pixel clock. Likewise, we fail to find any motivation, suggestion or teaching in the applied prior art that would have made it obvious at the time the invention was made to a person of ordinary skill in the art to have obfuscated Cox's invention by maintaining the analog video outputs from the CMOS image sensors in analog format along the entire signal path from the CMOS image sensors to the display (i.e., by omitting the analog to digital conversion of the video signals and all of the digital processing thereof).

In our view, the only suggestion for modifying Cox in the manner proposed by the examiner to meet the above-noted limitations stems from hindsight knowledge derived from the appellants' own disclosure. The use of such hindsight knowledge to support an obviousness rejection under 35 U.S.C. § 103 is, of course, impermissible. See, for example, W. L. Gore and Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

For the reasons set forth above, the decision of the examiner to reject claim claims 7 to 13 under 35 U.S.C. § 103 is reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 7 to 13 under 35 U.S.C. § 103 is reversed.

REVERSED

NEAL E. ABRAMS Administrative Patent Judge	)
MICHAEL R. FLEMING Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
JEFFREY V. NASE Administrative Patent Judge	)

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