

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte KEVIN ZHANG

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Appeal No. 2004-1608  
Application 09/752,873

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HEARD: February 24, 2005

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Before JERRY SMITH, RUGGIERO, and MACDONALD, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 5, 6, 8-12 and 19-26, which constitute all the claims remaining in the application.

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The disclosed invention pertains to a method and apparatus for accessing a cache memory.

Representative claim 5 is reproduced as follows:

5. A cache data access system, comprising:

a plurality of ways;

decoders coupled to each of said ways, wherein each decoder is to find a data location in one said plurality of ways based on an address;

a tag unit to compare said address with a tag array and to generate a hit/miss signal; and

sense amplifiers coupled to each of said ways, wherein one of said sense amplifiers is to read data from said data location if it receives said hit/miss signal as a hit,

wherein said data read by the one of the sense amplifiers is transmitted on a global bitline.

The examiner relies on the following references:

Brauer et al. (Brauer)	5,550,774	Aug. 27, 1996
Ayukawa et al. (Ayukawa)	US2002/0118591	Aug. 29, 2002
	(effective filing date of Aug. 16, 1999)	

Claims 5, 6, 8-12 and 19-26 stand rejected under 35 U.S.C. § 103(a). As evidence of obviousness the examiner offers Brauer in view of Ayukawa.

Rather than repeat the arguments of appellant or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellant's arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 5,6,8-12, and 19-26. Accordingly, we affirm.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to

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modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See Id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). Only those arguments actually made by appellant have been considered in this decision.

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Arguments which appellant could have made but chose not to make in the briefs have not been considered and are deemed to be waived [see 37 CFR § 41.37(c)(1)(vii)(2004)].

Before we consider the merits of the rejection, we address appellant's argument that Ayukawa does not qualify as prior art against the appealed claims. Ayukawa is a United States application for patent which was published on August 29, 2002. The publication indicates that the application for patent is a continuation of a parent application filed on April 5, 2001 which parent application was a continuation of a grandparent application filed on August 16, 1999. Because the grandparent application was filed as a 371 application, appellant argues that the parent application is only entitled to the filing date of April 5, 2001 which is after the filing date of the present application [brief, page 3].

The examiner responds that the Ayukawa patent which issued from the grandparent application has an effective filing date of August 16, 1999 [answer, page 4]. Appellant responds that the Ayukawa patent is not the document which was used in the

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rejection. Appellant reiterates his position that the use of the Ayukawa publication is procedurally defective [reply brief, page 1].

We disagree with appellant's position that the Ayukawa publication is not entitled to the filing date of the grandparent application. We have before us the situation where a published United States patent application relies on a chain of United States continuing applications resulting from an international application filed on February 17, 1997. This situation is covered in the Manual of Patent Examining Procedure (MPEP) at section 1896 in the section entitled "**References That Resulted From, or Claimed Benefit of, an International Application.**"

Since the international application was filed before November 29, 2000 and the published application claims priority benefits under 35 U.S.C. § 120, section (C)(3) of MPEP § 1896 applies. Section (C)(3) states the following:

For U.S. application publications of applications that claim the benefit under 35 U.S.C. 120 or 365(c) of an international application filed prior to November 29, 2000, apply the reference under 35 U.S.C. 102(e) as of the actual filing date of the later-filed U.S. application that claimed the benefit of the international application.

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Therefore, the Ayukawa publication is entitled to the actual filing date of the grandparent application that claimed the benefit of the international application which is August 16, 1999. Since August 16, 1999 is before the filing date of appellant's application, Ayukawa does qualify as prior art against the claims on appeal.

The examiner's rejection is set forth in the final rejection which has been incorporated into the answer at page 4. The examiner essentially finds that Brauer teaches the claimed cache memory except that Brauer does not teach the claimed global bitline. The examiner cites Ayukawa as teaching a global bitline in a cache environment. The examiner finds that it would have been obvious to the artisan to use a global bitline in Brauer for the advantages taught by Ayukawa.

As a general argument, appellant notes that the claimed invention uses a global bitline which eliminates the need for a multiplexer as used in Brauer. Appellant argues that the artisan would not have been motivated to modify the disclosure of Brauer with the global bitline of Ayukawa. Specifically, appellant argues that nothing in Brauer suggests that the multiplexer is not required, and that the cache in Ayukawa is not an associative cache like the cache in Brauer. Appellant argues that the

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motivation proposed by the examiner is based on hindsight gleaned from appellant's own disclosure [brief, pages 3-5].

With respect to claims 5, 8 and 21, which stand or fall together [brief, page 2], appellant specifically argues that there is no motivation to combine the references. The examiner responds that Ayukawa clearly suggests that global bitlines are desirable in cache devices for at least the reason of faster accessing speed and reduction in circuitry and complexity [answer, pages 5-7]. Appellant responds that the examiner has not identified any motivation to combine the teachings of Brauer and Ayukawa which comes from the references themselves [reply brief, pages 1-3].

We will sustain the examiner's rejection of claims 5, 8 and 21. Ayukawa teaches a cache memory in which a global bitline is provided for four bitline pairs [page 5, paragraph 94]. Regardless of whether the cache memory of Ayukawa is an associative cache or a direct cache, we find that Ayukawa teaches that four bitlines of a cache can be connected to a single global bitline. Note also that Ayukawa teaches how a plurality of sense amplifiers can be connected to global bitlines [page 11, paragraph 171]. Ayukawa also teaches that the global bitlines can be disposed with respect to power lines so that the chip size

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can be reduced [page 7, paragraphs 14-15]. Therefore, we agree with the examiner that Ayukawa provides motivation for modifying the cache of Brauer. Specifically, Ayukawa would have taught the artisan that using global bitlines in Brauer would enable a reduction in chip size which is always a desirable result in integrated circuit devices.

With respect to claims 6, 9-11 and 25, which stand or fall together, appellant argues that the examiner fails to make a prima facie case of obviousness because the examiner fails to identify what portions of the references are relied upon for the combination of local sensing and subsequent global transmitting by the sense amplifiers [brief, pages 5-6]. The examiner responds that local sensing, local bitlines and global bitlines are shown in Ayukawa [answer, page 7]. Appellant responds that the examiner has failed to identify the pertinent portions of the applied prior art with particularity [reply brief, page 3].

We will sustain the examiner's rejection of claims 6, 9-11 and 25. As noted by the examiner, Ayukawa teaches in Figure 5 that local bitlines DL connect the sense amplifiers SA to the various banks of memory. When the teachings of Ayukawa are combined with the teachings of Brauer, the local bitlines would

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connect the sense amplifiers to each of the ways of Brauer as claimed.

With respect to separately argued claim 12, appellant argues that the examiner fails to address the recitations of claim 12 at all [brief, page 6]. The examiner responds that appellant does not identify a particular feature of claim 12, but the examiner points to the hit signals of Brauer [answer, page 7]. Appellant responds that the examiner has failed to meet his initial burden of presenting a prima facie case of obviousness. Appellant asserts that the examiner has failed to identify how the steps of providing data and generating the hit signal occur at the same time [reply brief, page 3].

We will sustain the examiner's rejection of claim 12. Although the examiner did not specifically point out where in the applied prior art the claimed feature is taught, we find that the feature recited in claim 12 is taught by Brauer. Specifically, Brauer teaches that each of the four data arrays couples its selected cache line to its bitlines, and simultaneously, the four tag arrays output four tags to the comparators [column 4, lines 15-20]. We find that this teaching suggests that the steps of providing data and generating a hit signal occur at the same time in Brauer.

With respect to claims 19, 20 and 26, which stand or fall together, appellant again argues that the examiner has failed to address the recitations of these claims [brief, page 6]. The examiner responds that global bitlines are shown in Ayukawa [answer, page 7]. Appellant responds that the examiner has failed to meet his initial burden of presenting a prima facie case of obviousness. Appellant asserts that the examiner has ignored that these claims recite a global receiver [reply brief, page 4].

We will sustain the examiner's rejection of claims 19, 20 and 26. The global bitline GBL of Ayukawa is clearly connected to a global receiver MA [see Figure 13, for example, and accompanying description].

With respect to separately argued claim 22, appellant again argues that the examiner has failed to address the recitations of these claims [brief, page 6]. The examiner responds that Ayukawa teaches a controller BKCONTH responsive to a hit signal for controlling a sense amplifier [answer, pages 7-8]. Appellant responds that the examiner has failed to meet his initial burden of presenting a prima facie case of obviousness. Appellant asserts that the examiner has failed to identify how

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the cited references teach an address decode unit as claimed [reply brief, page 4].

We will sustain the examiner's rejection of claim 22. We agree with the examiner that Ayukawa teaches the selection of one of the sense amplifiers in response to the hit signals. We find that this operation constitutes an address decode unit as broadly recited in claim 22.

With respect to claims 23 and 24, which stand or fall together, appellant again argues that the examiner has failed to address the recitations of these claims [brief, page 6]. The examiner responds that Brauer teaches decoders, tag arrays, hit signals and sense amplifiers [answer, page 8]. Appellant responds that the examiner has failed to meet his initial burden of presenting a prima facie case of obviousness. Appellant asserts that the examiner has failed to identify how the cited references teach the recitations of these claims [reply brief, pages 4-5].

We will sustain the examiner's rejection of claims 23 and 24. We agree with the examiner that Ayukawa teaches that there is a separate address decode unit for each of the banks of memory. Since each decode unit has a decoder and a control unit arranged in the claimed manner, we find that the collective

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teachings of Brauer and Ayukawa suggest a plurality of decoders, a tag unit and a plurality of control units connected together in the manner recited in claim 23.

In summary, we have sustained the examiner's rejection with respect to each of the claims on appeal. Therefore, the decision of the examiner rejecting claims 5, 6, 8-12 and 19-26 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

JERRY SMITH	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
JOSEPH F. RUGGIERO	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
	)	INTERFERENCES
	)	
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