

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte STEPHEN L. BASS and ROHIT BHATIA

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Appeal No. 2004-1629  
Application No. 09/507,204

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ON BRIEF

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Before THOMAS, KRASS and SAADAT, Administrative Patent Judges.  
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1-21, which are all of the claims pending in this application.

We reverse.

BACKGROUND

Appellants' invention is directed to a method and apparatus for maximizing instruction execution efficiency of a microprocessor's pipeline data by preserving the stalled data. In speed critical pipeline stages, the data is stored in a deferred stall register after the data is allowed to propagate



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We make reference to the answer (Paper No. 15, mailed February 10, 2004) for the Examiner's reasoning, and to the appeal brief (Paper No. 14, filed November 12, 2003) and the reply brief (Paper No. 16, filed April 8, 2004) for Appellants' arguments thereagainst.

OPINION

With respect to the 35 U.S.C. § 102 rejection of claims 1, 3, 4, 7, 8, 10-14, 17, 18 and 21 as anticipated by McLellan, Appellants point out that the prior art begins capturing data in a queue stage immediately after a stall is initiated whereas the claims allow data that is to be stalled to propagate through N more stages before storing the data (brief, page 10). Appellants further assert that if the queue stage 16 of McLellan (Figure 1) is equated with claimed "N more stage," then the reference lacks a "stall register" for capturing the output from the "N more stages" (brief, page 10). On the other hand, Appellants argue that if the queue stage 16 of McLellan is characterized as the claimed "deferred stall register," then the reference does not allow data to propagate through "N more stages" and instead, is clocked into the queue stage (brief, page 10; reply brief, page 2).

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In response to Appellants' arguments, the Examiner asserts that McLellan does indeed provide for an "N cycle wait" by teaching that "once a stall is initiated, data begins capturing in a queue stage immediately" (answer, page 15). The Examiner argues that "*immediately* means that data is captured at the start of the **next** clock cycle after the stall is initiated" or if N=1, there is one cycle wait between the time that the stall is initiated and when data begins (*id.*). The Examiner further explains that data from stage 3 will go N more stages from stage 3 to the Q-stage when N=1 (answer, pages 17).

A rejection for anticipation under section 102 requires that the four corners of a single prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. See Atlas Powder Co. v. Ireco Inc., 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999); In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

After reviewing McLellan, we agree with Appellants' assertion that the queue stage of the prior art cannot be equated to both the claimed "N more stages" and "stall register." McLellan relates to a pipelines computer system in which a queue

stage receives the output of one stage when a stall occurs in the next stage (abstract). Queue stage 16 is asserted when a pipeline stall occurs in stage 4 or downstream during which stage 3 sends its output to the queue stage 16 to avoid stalling the earlier pipeline stages (col. 5, lines 51-58). As depicted in Figure 1 of McLellan, the position of queue stage 16 is such that if  $N=1$ , the stalled data must be propagated one more stage to queue stage 16, which becomes the "last of the  $N$  more stages" and its data must be stored in a deferred stall register. Here the data is already in queue stage 16 which cannot read on a stall register to send the data output from the "last of the  $N$  more stages." For queue stage 16 to be a stall register after the data is propagated at least one more stage, the stall must have occurred in stage 2 or 1 which after one or two more stages the data is stored in queue stage 16. However, in this case the data output from queue stage 16 to stage 4 is not delayed by 1 or more cycles and is sent to stage 4 without delay as soon as the stall is removed.

Therefore, what the Examiner characterizes in McLellan as the stall register and the propagation of the data after a stall is initiated, cannot read on all of the claimed steps. Thus, McLellan does not anticipate the claimed subject matter and the

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35 U.S.C. § 102 rejection of claims 1, 3, 4, 7, 8, 10-14, 17, 18 and 21 over McLellan cannot be sustained.

With respect to the rejection of claims 2, 5, 6, 9, 19 and 20, the Examiner modifies McLellan by moving the relative position of the stall register and further relies on Peatman for disclosing the use of binary counters in rejecting claims 15 and 16 (answer, pages 12-15). However, in discussing these modifications, the Examiner has pointed to no additional teaching that would have overcome the deficiencies of McLellan as discussed above with respect to the independent claims 1 and 7. Therefore, the 35 U.S.C. § 103 rejection of claims 2, 5, 6, 9, 19 and 20 over McLellan and of claims 15 and 16 over McLellan and Peatman cannot be sustained.

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CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1, 3, 4, 7, 8, 10-14, 17, 18 and 21 under 35 U.S.C. § 102 and of claims 2, 5, 6, 9, 15, 16, 19 and 20 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS	)	
Administrative Patent Judge	)	
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	)	
	)	BOARD OF PATENT
ERROL A. KRASS	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
	)	
MAHSHID D. SAADAT	)	
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