

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* DAVID F. TOBIAS, RICHARD G. RUSSELL and MARK T. ELLIS

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Appeal No. 2004-1716  
Application 10/106,631

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ON BRIEF

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Before HAIRSTON, KRASS and OWENS, *Administrative Patent Judges*.  
OWENS, *Administrative Patent Judge*.

*DECISION ON APPEAL*

This appeal is from the final rejection of claims 2-9, which are all of the claims pending in the application.

*THE INVENTION*

The appellants claim a microcontroller having a means for defining a scan path comprising a peripheral device's

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configuration registers. Claim 2 is illustrative:

2. A microcontroller, comprising:

an execution unit;

a peripheral device coupled to the execution unit, the peripheral device comprising configuration registers; and

a means for defining a scan path comprising the configuration registers and for communicating configuration data for the peripheral device.

*THE REFERENCE*

Byers et al. (Byers)                      5,168,555                      Dec. 1, 1992

*THE REJECTION*

Claims 2-9 stand rejected under 35 U.S.C. § 103 as being unpatentable over Byers.

*OPINION*

We reverse the aforementioned rejection. We need to address only the sole independent claim, i.e., claim 2.

Byers discloses (col. 4, lines 11-27):

The program information on bus **66** enters the controller **52** at unit support logic **68** and is applied to the scan set logic **68** to provide output signals on line **69** for setting the individual interface latches **71**, **72** and **73** of the MSU [memory storage unit] to MSU interfaces A, B and C. The signals circulate via lines **69** to the input of partitioning register **75** and via line **76** to the input of system status register **65**. The return path of the series scan set configuration signals is shown as line return path **77**. Once the latches representing the partitioning register **75** bit positions and the system

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status register **65** bit positions are dynamically established, then the scan set logic **68** informs the system support processor **54**. Then the information in partitioning register **75** is transferred via bus **74** to the input logic of latches **71**, **72** and **73** to set the interface latches.

The examiner argues that "Byers's combine[d] teachings of 71-73, 68 & 75, as a single collective, teaches the above argued claim limitations (e.g., 'a means for defining a scan path comprising the configuration registers and for communicating configuration data for the peripheral device[')]", and that "the Byers- 'interface latches 71, 72 and 73 of the MSU' represents/equates the claimed 'configuration registers'; and the Byers - a collective combination of '77, 75 & 65' represents/equates the claimed 'means for defining a scan path and for communicating configuration data for the peripheral device'; and the Byers- '52' MSU represents/equates the claimed 'peripheral device'" (answer, page 5).

The appellants' claim 2, however, does not only require a peripheral device's configuration registers and a means for defining a scan path, but also requires that the scan path comprises the configuration registers. As set forth above, Byers discloses that after the scan path has been used to establish the bit positions of partitioning register 75 and system status

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register 65, then information in partitioning register 75 is transferred via bus 74 to the input logic of interface latches 71-73, which the examiner relies upon as corresponding to the appellants' configuration registers, to set those latches. This disclosure indicates that latches 71-73 are not in the scan path. The examiner has not provided evidence or reasoning to the contrary, or explained how Byers would have fairly suggested, to one of ordinary skill in the art, placing latches 71-73 in the scan path.

Accordingly, we conclude that the examiner has not carried the burden of establishing a *prima facie* case of obviousness of the appellants' claimed invention.

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*DECISION*

The rejection of claims 2-9 under 35 U.S.C. § 103 over Byers  
is reversed.

*REVERSED*

	)	
KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
	)	
	)	
	)	BOARD OF PATENT
ERROL A. KRASS	)	
Administrative Patent Judge	)	APPEALS AND
	)	
	)	INTERFERENCES
	)	
TERRY J. OWENS	)	
Administrative Patent Judge	)	

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